(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 October 2003 (23.10.2003)

PCT

(10) International Publication Number
WO 03/088316 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US03/11417

(22) International Filing Date: 11 April 2003 (11.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/372,263	12 April 2002 (12.04.2002)	US
60/382,133	21 May 2002 (21.05.2002)	US
60/387,826	8 June 2002 (08.06.2002)	US
60/398,316	24 July 2002 (24.07.2002)	US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 03/088316 A2

(54) Title: ELECTROPOLISHING AND ELECTROPLATING METHODS

(57) Abstract: In one aspect of the present invention, an exemplary method is provided for electroplating a conductive film on a wafer. The method includes electroplating a metal film on a semiconductor structure having recessed regions and non-recessed region within a first current density range before the metal layer is planar above recessed regions of a first density, and electroplating within a second current density range after the metal layer is planar above the recessed regions. The second current density range is greater than the first current density range. In one example, the method further includes electroplating in the second current density range until the metal layer is planar above recessed regions of a second density, the second density being greater than the first density, and electroplating within a third current density range thereafter.

ELECTROPOLISHING AND ELECTROPLATING METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority of earlier filed provisional applications U.S. Application Nos. 60/372,263, entitled "ENHANCING SURFACE ROUGHNESS AFTER ELECTROPOLISHING," filed on April 12, 2002; No. 60/382,133, entitled "METHOD FOR REDUCING RECESS IN COPPER ELECTROPOLISHING," filed on May 21, 2002; No. 60/387,826, entitled "METHOD TO PLATE PLANAR METAL FILM ON SEMICONDUCTOR WAFERS," filed on June 8, 2002; No. 60/398,316, entitled "METHOD FOR REDUCING RECESS NON-UNIFORMITY ON PATTERNED TRENCH OR PAD AREA IN ELECTROPOLISHING PROCESS," filed on July 24, 2002, all of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field:

[0002] This invention relates generally to semiconductor processing methods, and more particularly to electropolishing and electroplating methods for electropolishing and electroplating conductive layers on semiconductor devices.

2. Description of the Related Art:

[0003] Semiconductor devices are manufactured or fabricated on semiconductor wafers using a number of different processing steps to create transistor and interconnection elements. To electrically connect transistor terminals associated with the semiconductor wafer, conductive (e.g., metal) trenches, vias, and the like are formed in dielectric materials as part of the semiconductor device. The trenches and vias couple electrical signals and power between transistors, internal circuit of the semiconductor devices, and circuits external to the semiconductor device.

[0004] In forming the interconnection elements the semiconductor wafer may undergo, for example, masking, etching, and deposition processes to form the desired electronic circuitry of the semiconductor devices. In particular, multiple masking and etching steps can be performed to form a pattern of recessed areas in a dielectric layer on a semiconductor wafer that serve as trenches and vias for the interconnections. A deposition process may then be performed to deposit a metal layer over the semiconductor wafer thereby depositing metal both in the trenches and vias and also on the non-recessed areas of the semiconductor wafer. To isolate the interconnections, such as patterned trenches and vias, the metal deposited on the non-recessed areas of the semiconductor wafer is removed.

[0005] Conventional methods of removing the metal film deposited on the non-recessed areas of the dielectric layer on the semiconductor wafer include, for example, chemical mechanical polishing (CMP). CMP methods are widely used in the semiconductor industry to polish and planarize the metal layer within the trenches and vias with the non-recessed areas of the dielectric layer to form interconnection lines.

[0006] In a CMP process, a wafer assembly is positioned on a CMP pad located on a platen or web. The wafer assembly includes a substrate having one or more layers and/or features, such as interconnection elements formed in a dielectric layer. A force is then applied to press the wafer assembly against the CMP pad. The CMP pad and the substrate assembly are moved against and relative to one another while applying the force to polish and planarize the surface of the wafer. A polishing solution, often referred to as polishing slurry, is dispensed on the CMP pad to facilitate the polishing. The polishing slurry typically contains an abrasive and is chemically reactive to selectively remove from the wafer the unwanted material, for example, a metal layer, more rapidly than other materials, for example, a dielectric material.

[0007] CMP methods, however, can have several deleterious effects on the underlying semiconductor structure because of the relatively strong mechanical forces involved. For example, as interconnection geometries move to 0.13 microns and below, there can exist a large difference between the mechanical properties of the conductive materials, for example copper and the low k films used in typical damascene processes. For instance, the Young Modulus of a low k dielectric film may be greater than 10 orders of magnitude lower than that of copper. Consequently, the relatively strong mechanical force applied on the dielectric films and copper in a CMP process, among other things, can cause stress related defects on the semiconductor structure that include delamination, dishing, erosion, film lifting, scratching, or the like.

[0008] Another method for removing metal films deposited on the non-recessed areas of the dielectric layer includes electropolishing. However, because of the isotropic nature and poor planarization efficiency of electropolishing, the surface of the metal film topology is desirably planar to prevent recesses and the like that may degrade device performance.

[0009] New processing techniques for depositing and removing metal layers are desired. For example, a metal layer may be deposited or removed from a wafer using an electroplating or electropolishing process. In general, in an electroplating or electropolishing process the portion of the wafer to be plated or polished is immersed within an electrolyte fluid solution and an electric charge is then applied to the wafer. These conditions result in copper being deposited or removed from the wafer depending on the relative electrical charges.

BRIEF SUMMARY OF THE INVENTION

[0010] In one aspect of the present invention, an exemplary method is provided for electroplating a conductive film on a wafer. One exemplary method includes electroplating a metal film on a semiconductor structure having recessed regions and non-recessed regions. The method includes electroplating within a first current density range before the metal layer is planar above recessed regions of a first density. Further, electroplating within a second current density range after the metal layer is planar above the recessed regions, where the second current density range is greater than the first current density range. In one example, the method further includes electroplating in the second current density range until the metal layer is planar above recessed regions of a second density, the second density being greater than the first density, and electroplating within a third current density range thereafter.

[0011] The present invention is better understood upon consideration of the detailed description below in conjunction with the accompanying drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **Figs. 1A** and **1B** illustrate cross-sectional views of interconnect structures after metal plating and electropolishing respectively;

[0013] **Figs. 2A – 2C** illustrate cross-sectional views of a metal film profile during an exemplary metal plating process;

[0014] **Fig. 3** illustrates an exemplary relationship between hump size, leveler concentration, and plating current;

[0015] **Fig. 4** illustrates the relationship between plating current and hump size with and without leveler;

[0016] **Figs. 5A – 5C** illustrate cross-sectional views of metal film profiles during an exemplary metal plating process;

[0017] **Figs. 6A – 6C** illustrate cross-sectional views of metal film profiles during an exemplary metal plating process;

[0018] **Figs. 7A – 7C** illustrate cross-sectional views of metal film profiles during an exemplary metal plating process;

[0019] **Figs. 8A – 8C** illustrate cross-sectional views of metal film profiles during an exemplary metal plating process;

[0020] **Fig. 9** illustrates a cross-sectional view of an interconnect structure with a dummy structure;

[0021] **Figs. 10A** and **10B** illustrate cross-sectional views of a metal film profile during an exemplary metal plating process;

[0022] **Figs. 11A** and **11B** illustrate cross-sectional views of a metal film profile during an exemplary metal plating process;

[0023] **Figs. 12A – 12C** illustrate cross-sectional views of a metal film profile during an exemplary metal plating process;

[0024] **Figs. 13A – 13H** illustrate exemplary plating current sequences;

[0025] **Figs. 14A – 14C** illustrate plan views of various exemplary dummy structures;

[0026] **Figs. 15A – 15C** illustrate plan views of various exemplary dummy structures;

[0027] **Figs. 16A – 16C** illustrate plan views of various exemplary dummy structures;

[0028] **Figs. 17A – 17C** illustrate plan views of various exemplary dummy structures;

[0029] **Figs. 18A** and **18B** illustrate cross-sectional views of metal film profiles during exemplary metal plating processes;

[0030] **Figs. 19A-19F** illustrate an exemplary electropolishing process for a dual damascene structure;

[0031] **Figs. 20A-20D** illustrate an exemplary electropolishing process for a semiconductor structure;

[0032] **Figs. 21A-21D** illustrate exemplary metal layers of different grain sizes formed on semiconductor structures;

[0033] **Figs. 22A-22C** illustrate various exemplary images of a copper layer having a relatively large grain size;

[0034] **Figs. 23A-23C** illustrate various exemplary images of a copper layer having a relatively small grain size;

[0035] **Fig. 24** illustrates a graph showing a relationship between grain size and surface roughness of a copper layer after electropolishing;

[0036] **Figs. 25A-25D** illustrate a change in a metal layer grain size with respect to time;

[0037] **Fig. 26** illustrates a graph showing a general relationship of the metal layer grain size with respect to time;

[0038] **Fig. 27** illustrates a graph showing the general relationship of the grain growth rate with respect to the annealing temperature;

[0039] **Fig. 28A** illustrates an exemplary electropolishing apparatus;

[0040] **Fig. 28B** illustrates an exemplary process for electropolishing a wafer;

[0041] **Figs. 29A-29D** illustrate an exemplary process for electropolishing a portion of a wafer;

[0042] **Figs. 30A-30D** illustrate an exemplary process for electropolishing a semiconductor structure;

[0043] **Fig. 30E** illustrates an exemplary electropolished semiconductor structure having copper recesses;

[0044] **Fig. 31** illustrates an exemplary forward and reverse pulse waveform for an electropolishing method;

[0045] **Figs. 32A-32F** illustrate an exemplary electropolishing process including a forward and reverse pulse waveform; and

[0046] **Fig. 32G** illustrates an exemplary semiconductor structure electropolished with a forward and reverse pulse waveform.

DETAILED DESCRIPTION

[0047] In order to provide a more thorough understanding of the present invention, the following description sets forth numerous specific details, such as specific materials, parameters, and the like. It should be recognized, however, that the description is not intended as a limitation on the scope of the present invention, but is instead provided to enable a better description of the exemplary embodiments.

I. Method to Electroplate Planar Metal Films

[0048] According to one aspect, an exemplary method for plating planar metal films on semiconductor structures is described. The exemplary plating method includes plating a metal film with increased planarity over interconnect structures formed on semiconductor wafers, for example, with reduced hump or over-plating and dishing. Various exemplary plating methods are described for forming improved planar metal films on patterned semiconductor structures by using combinations of chemistry, plating process sequences, and/or adding dummy structures within interconnect structures.

[0049] The semiconductor industry generally uses copper in a damascene process to form metal interconnections in semiconductor devices. The damascene process patterns dielectric material with recessed regions and non-recessed regions as canal-like trenches and/or vias corresponding to

the desired interconnects. A barrier and seed layer may be deposited on the dielectric material structure followed by copper plated on the barrier and/or seed layer. Copper on the non-recessed regions is typically polished away by chemical mechanical polishing (CMP). CMP includes both chemical (ion exchange) and mechanical (stress) processes to remove the copper layer on the non-recessed regions leaving copper in the trenches and/or vias, i.e., the recessed regions. Pressure applied on the polished surface may result in oxide loss, erosion, metal delamination, and dielectric lifting.

[0050] In order to achieve significantly higher speed performance, copper is desirably integrated with low-k dielectrics and preferably with ultra-low-k dielectrics ($k<2.5$). The low-k dielectric implementation strategy typically used today gradually migrates from oxide ($k=4.0$) to fluorinated oxide ($k=3.5$), and then to the low-k dielectrics with successively lower k values of 3.0, 2.6, 2.2, and finally, k values of less than 2.0. The multi-step low-k implementation strategy described above is very costly, carries high risk, and gives IC manufacturers a great deal of uncertainty for the success of device manufacturability. Since each generation of low-k dielectric has its own mechanical properties and integration characteristics, IC manufacturers are required to develop new CMP and other related processes when migrating from one generation to the next. Tool and process extendibility, manufacturing yield, and device reliability have become major concerns in the industry because with each new manufacturing mode, IC manufacturers must change low-k dielectric materials and processes.

[0051] An exemplary process that reduces the mechanical damage to low-k dielectric structures includes electropolishing. An exemplary electropolishing process is described in U.S. Patent No. 6,395,152, entitled METHODS AND APPARATUS FOR ELECTROPOLISHING METAL INTERCONNECTIONS ON SEMICONDUCTOR DEVICES, filed on July 2, 1999, which is incorporated in its entirety by reference herein. To improve electropolishing processes, however, it is desired to increase the planarity of the deposited metal film.

[0052] An exemplary profile of a copper film **104** plated by a conventional plating process on a damascene structure is shown in **Fig. 1A**. The semiconductor structure includes a dielectric layer **108** formed over a wafer **100** or previously formed semiconductor device structure. The structure may further include a barrier layer **106** and other materials known in the art. The structure includes a pattern of recessed regions **101r** and non-recessed regions **101n** corresponding to trenches and/or vias separated by dielectric layer **108**. Metal or copper layer **104** is formed over the structure filling the recessed regions **101r** and formed over the non-recessed regions **101n**. The underlying structure typically results in a non-planar surface topology of copper layer **104** located over structures in dielectric layer **108**. For example, the non-planar topology may include a hump **102** and recess **110** corresponding generally to the underlying densely spaced recessed regions **101r** and

wide opening recessed regions respectively. Hump **102**, recess **110**, and other non-planar features may be caused, for example, by the plating chemistry in an electroplating process.

[0053] **Fig. 1B** illustrates the structure of **Fig. 1A** after an electropolishing process. Metal layer **104** is typically polished back to the surface of the non-recessed areas such that metal layer **104** within the recessed regions **101r**, i.e., the trenches and vias, is isolated from adjacent recessed regions **101r**. As shown in **Fig. 1B**, hump **102** may remain at least partially over the dense pattern area and dishing, shown by recessed region **110**, may remain after electro-polishing due to the isotropic nature of the electropolishing. Humps and recesses may degrade the performance of the formed devices. For example, a hump left above densely spaced trenches or vias may cause an electrical short circuit between adjacent lines and recesses may result in the reduction of the conductance of the formed interconnection lines. Plating a planar metal layer **104** may reduce humps and recesses and improve device performance.

[0054] **Figs. 2A-2C** illustrate an exemplary electroplating process over time for plating copper layer **204** over a dielectric layer **208** having a plurality of densely spaced recessed regions **210r** and non-recessed regions **210n**. In general, a plating bath includes three main additives, e.g., an accelerator, a suppressor, and a leveler. The primary function of the accelerator is to enhance the plating process within recessed regions; the primary function of suppressor is to suppress the plating process on the shoulder of the recessed regions; and the primary function of leveler is to level the surface profile of the plated film, mostly to level hump **202**. The combination of accelerator and suppressor results in the super fill or bottom fill as illustrated in **Fig. 2A**. More particularly, the plating rate at the bottom of the trench or recessed region **210r** is significantly higher than at the top and shoulder of the recessed region **210r**. However, when trenches or vias are filled up, the chemicals in the trench region will continue to enhance the plating rate resulting in humps **202** as shown in **Fig. 2B**, which may run together over time to form a larger hump **202** as shown in **Fig. 2C**.

[0055] **Fig. 3** illustrates a relationship between leveler concentration and relative hump height (often referred to as the "over-plating burden") at increasing plating currents **394**, **392**, and **390**. The relationship suggests that hump size may be reduced with sufficient concentrations of leveler and increased plating currents as shown in the graph as leveler concentration increases.

[0056] **Fig. 4** further shows a relationship between the plating current and hump size with leveler **498** and without leveler **496**. As can be seen, the instance with leveler **498** may reduce the hump size at most plating currents. However, at large plating currents a hump may still occur despite leveler **498**. Further, hump size is relatively greater at all currents without leveler.

[0057] **Figs. 5A – 5C** show the profiles of metal film **504** over time during an exemplary plating process at a relatively small plating current I_1. The exemplary process includes directing electrolyte fluid at a rotating chuck holding a wafer, but as will be recognized, other methods such as immersion and the like may be used. The rotating chuck may rotate at a speed in the range of, e.g., 50-200 rpm, and preferably 125 rpm. A planar metal film **504** can be plated under the following exemplary process conditions:

Chemistry: Electrolyte fluid such as ViaForm manufactured by Enthone-OMI

Accelerator: 1.5 to 2.5 ml/liter, preferably 2 ml/liter

Suppressor: 7 to 9 ml/liter, preferably: 8 mi/liter

Leveler: 1.25 to 1.75 ml/liter, preferably: 1.5 ml/liter

Copper: 16 to 20 gram/liter, preferably, 17.5 gram/liter

Sulfuric Acid: 150 to 200 gram/liter, preferably 175 gram/liter

Rotation speed of wafer: 50 to 200 rpm, preferably 125 rpm

Current density: 0.5 to 5 mÅ/cm^2, preferably 2 mÅ/cm^2

[0058] The exemplary process plates copper layer **504** over dielectric layer **508**, filling the recessed regions **510r** and non-recessed regions **510n** relatively quickly as seen at t_1. At a time t_2, where t_2 is greater than t_1, recessed regions **510r** are filled and metal layer **504** is relatively planar above the recessed and non-recessed regions **510r** and **510n** of dielectric layer **508**. At a time t_3, where t_3 is greater than t_2, the exemplary process continues to plate metal layer **504** at a constant rate above recessed regions **510r** and non-recessed regions **510n** to create a planar metal layer **504** of a desired height above the structure.

[0059] **Figs. 6A – 6C** show exemplary profiles of a metal film during a similar plating process, but at a relatively larger plating current than the process of **Figs. 5A – 5C**. The plating current density I_2 is in the range of 5mÅ/cm^2 to 30 mÅ/cm^2, for example. The exemplary process at the relatively larger plating current produces humps **602** over recessed regions **610r** at t_2. The humps **602** may grow together to form a larger hump **602** at t_3.

[0060] **Figs. 7A – 7C** show exemplary profiles of a metal film profile during another exemplary metal plating process. As shown in **Figs. 7A** and **7B**, the plating process is conducted at a relatively smaller current I_1 similar to **Figs. 5A-5C** up to process time t_2 to produce a hump free profile of metal layer **704**. The plating current may thereafter be increased to I_2 and plated to time t_3, as illustrated in **Fig. 7C**, to a desired thickness of metal layer **704**. The exemplary two-step plating process can achieve a planar metal film **704**. In this exemplary process, the trenches or vias are fully

plated to form a planar metal film **704** before increasing the current to a level where humps will form. For example, if the trenches or vias are not fully plated when the current is increased, a hump may appear above recessed region **7010r** as the current is increased. **Figs. 8A – 8C** illustrate a metal film profile during a metal plating process where the plating current is increased to I_2 before the recessed regions **810r** are filled. As shown in **Fig. 8B**, the small hump **802** develops due to the large plating current I_2. As the process continues to plate copper film at large current I_2, the small individual humps grow into a large singular hump **802** as shown in **Fig. 8C**. It should be recognized that the current from t_1 to t_2 need not be constant and/or increase stepwise, but may increase smoothly during time t_1 to t_2.

[0061] Referring again to **Fig. 1A** a structure with high-density small trenches/vias and a large size trench and/or pad is shown. Due to the relatively large open area of recessed region **101r** shown to the right, which may include a trench and/or pad compared to the more narrow, densely spaced recessed regions **101r** shown to the left, the plating profile may include dishing **110** as described above. In one exemplary plating method, dummy structure **980** can be added inside the recessed region **911r**, e.g., a trench and/or pad area, as shown in **Fig. 9**. A detailed discussion of exemplary dummy structures may be found in U.S. Patent Application Serial No. 10/108,614, entitled ELECTROPLISHING METAL LAYERS ON WAFERS HAVING TRENCHES OR VIAS WITH DUMMY STRUCTURES, filed on March 27, 2002, which is incorporated in its entirety by reference herein.

[0062] **Figs. 10A** and **10B** show cross-sectional views of a plating profile during an exemplary plating process at a constant current over time. In this instance, the plating process uses a relatively small current and leveler resulting in a flat profile above the relatively dense trench or vias **1010r**. The dummy structure area **1080**, however, has more area to be plated resulting in a slight dishing **1020** of the final plating profile. The slight dishing **1020** will likely remain in the final profile after a subsequent electropolishing process as described above. Therefore, it is desirable to have a process that can plate a planar film on both densely spaced recessed regions **1010r** and the large trench area with dummy structure **1080**. The size of dense trench or via region **1010r** can be in the range of 0.035 to 0.5 micron with spacing between the trench or between the via in the range of 0.035 to 0.5 micron. The dummy structure **1080** size may be in the range of 0.05 to 2.0 micron with space in the range of 0.05 to 2.0 micron, preferably 0.5 micron. Generally, the dummy structure should be designed with relatively small size and larger space to minimize the copper loss in the trenches.

[0063] **Figs. 11A** and **11B** show cross-sectional views of a plating profile during an exemplary plating process including varying the current over time. The structure includes dummy structure **1180** formed at space w_1 and w_2, where $w_1 = w_2$. Copper film **1104** is plated at a relatively lower

plating current I_1 until dense recessed regions **1110r** are filled as shown in **Fig. 11A**. Recesses **1120** are formed in the relatively wider trenches/pad regions. The process continues to plate copper at a relatively higher plating current I_2, i.e., where $I_2 > I_1$, and a hump will grow from dishing **1120** such that the hump effect offsets the dishing to plate a planar surface as shown in **Fig. 11B**. A hump does not form above the dense recessed regions **1110r** because the dense trenches or vias have already been filled during the first portion of the process by using the relatively small plating current I_1. The two-step plating process results in a more planar profile of metal layer **1104** above the densely spaced recessed regions **1110r** and the large trench and/or pad area having dummy structure **1180** formed therein.

[0064] **Figs. 18A** and **18B** show cross-sectional views of metal film profiles over exemplary dummy structures. The ratio of the depth H of a trench and/or pad to dummy structure space or width W between structures may be varied to increase the planarity of a metal film. In general, the ratio of trench and/or pad height to dummy structure space is in the range of 0.3 to 2.0, and preferably 1. A deep trench will have a tendency to have more hump **1802** as shown in **Fig. 18B**, which will be used to balance the dishing **1810** for a wide space dummy structure, whereas a shallow trench will have a tendency to have less hump **1802** as shown in **Fig. 18A**.

[0065] **Figs. 12A – 12C** show cross-sectional views of a plating profile during an exemplary plating process that varies the current over time. The interconnect structure in dielectric layer **1208** is similar to that shown in **Figs. 11A** and **11B**, except that dummy structure **1280** is placed within the large trench or pad **1209**, **1211** at space w_1 and space w_2, where $w_2 > w_1$. An exemplary three-step plating process is described to plate a planar metal film **1204**, e.g., that is hump-free and dishing-free, on densely spaced recessed regions **1210r** and wide trench regions **1209** and **1211** adjacent dummy structure **1280**. The exemplary process through times t_1 and t_2 are similar to those previously described in **Figs. 11A** and **11B** with respect to increasing the current to create a planar topology above narrow recessed regions **1210r** and narrow space w_1.

[0066] At t_2, space w_2 still has dishing **1220** as shown in **Fig. 12A**. The current is further increased to I_3 to plate above w_2. In particular, the process increases the plating current from I_2 to I_3 to fill the recess **1220** and continues to plate the structure through t_3. Since the recessed region **1210r** and **1209** have been previously filled with metal layer **1204** at t_1 and t_2, the large current I_3 will not create a hump above these regions. The large plating current I_3 will create a hump above trench **1211** because trench **1211** was not fully filled before the plating process increases the current to I_3, as illustrated in **Fig. 12B**. I_3 may be varied depending on the plating process, size of trench **1211**, and the like such that the hump created will sufficiently offset the dishing in trench **1211** formed during t_1 and t_2.

[0067] Figs. 13A – 13H show various exemplary plating current sequences over time that may be used to achieve a planar metal layer. The exemplary plating current sequences including both current level and timing may be adjusted according to the size, spacing, and density of trenches and vias as well as the size and space of a dummy structure. Generally, the current sequence over time is controlled such that the effects of hump and dishing during plating balance or offset each other to create a planar metal layer surface. The plating current can be linear as shown in Fig. 13A, non-linear, i.e., curved, as shown in Figs. 13D-13H, or any combination of linear and non-linear segments over time. Further, the current sequences may decrease over periods of time as shown in Figs. 13G and 13H. In general, the plating current begins at a relatively small current and grows larger as the plating process progresses. In addition, the plating power supply can be run in constant voltage mode. In the present exemplary embodiment, the above description can change from current to voltage or to pulse power supply. A variety of pulse waveforms may be used such as bipolar pulse, modified sine-wave, unipolar pulse, pulse reverse, pulse on pulse, and duplex pulse. Exemplary pulse wave forms are described in U.S. Patent No. 6,395,152, entitled METHODS AND APPARATUS FOR ELECTROPOLISHING METAL INTERCONNECTIONS ON SEMICONDUCTOR DEVICES, filed on July 2, 1999, which is incorporated in its entirety by reference herein.

[0068] Figs. 14A – 14C are plan views of various exemplary dummy structures. Dummy structure may include a metal plug 1420 placed outside the trench, or the pad area, often referred to as the open area or field area, as shown in Fig. 14A. Alternatively, dielectric slots 1430 can be placed inside the large trench and/or pad area 1404, or dielectric dots 1450 can be placed inside the large trench and/or pad area 1404 as shown in Figs. 14B and 14C.

[0069] Figs. 15A – 15C are plan views of additional exemplary dummy structures that may be included in relatively large vias or recessed regions. Metal plug dummy structure in Fig. 15A is similar to that illustrated in Fig. 14A, except the metal plug column 1522 is shifted lower relatively to metal column 1520. Metal plug dummy structure in Fig. 15B is similar to that shown in Fig. 15A, except metal plugs 1520 and 1522 are rotated 45 degrees, which may reduce the inductance and capacitance of metal plug 1520 and 1522. Dielectric dots 1550 that are placed inside the large trench and/or pad area 1504 as shown in Fig. 15C are similar to those illustrated in Fig. 14C, except that dielectric dots 1550 are rotated 45 degrees and individual columns are shifted lower relative to adjacent column of dielectric dots 1550. The size and spacing may be adjusted depending on the particular application and the like.

[0070] Figs. 16A – 16C are plan views of additional exemplary dummy structures. Metal plug dummy structure as shown in Fig. 16A is similar to those illustrated in Fig. 14A, except the metal

plug column **1622** is shifted at an angle α. The angle α may be in the range of approximately 5 to 85 degrees, and preferably about 25 degrees. Dielectric slots **1630** as shown in **Fig. 16B** are similar to those illustrated in **Fig. 14B**, except that the dielectric slots **1630** are disconnected from each other in order to enhance the conductance of copper trench and/or pad **1604**. Dielectric dots **1650** placed inside the large trench and/or pad area **1604** as shown in **Fig. 16B** are similar to those illustrated in **Fig. 14C**, except that dielectric dots **1650** are rotated 45 degrees. It should be recognized that the rotation angle of dielectric dots **1650** may be in the range of 0 to 90 degrees, and further that that dielectric dots **1650** may be shaped as squares, rectangles, circles, and the like.

[0071] **Fig. 17A – 17C** are plan views of additional exemplary dummy structures. Metal plug dummy structures **1720** and **1722** as shown in **Fig. 17A** are similar to those illustrated in **Fig. 14A**, except the metal plug **1722** and **1722** are rotated about 45 degrees. Metal plugs **1722** and **1722** may be rotated between 0 and 90 degrees, and may be rotated at various degrees within a single structure. Dielectric slots **1730** as shown in **Fig. 17B** are similar to those illustrated in **Fig. 16B**, except that the dielectric slots **1730** are disconnected at similar locations along the horizontal direction. Dielectric dots **1750** placed inside the large trench and/or pad area **1704** as shown in **Fig. 17C** are similar to those illustrated in **Fig. 14C**, except that dielectric dots **1750** are shifted lower relative to adjacent columns of dielectric dots **1750**.

[0072] Although exemplary plating processes have been described with respect to certain embodiments, examples, and applications, it will be apparent to those skilled in the art that various modifications and changes may be made without departing from the invention. For example, various described methods may be used alone or in combination to electroplate planar metal films.

II. Method for Reducing Recess in Electropolishing

[0073] According to another aspect, an exemplary method for reducing the recess in a metal trench or metal pad after an electropolishing process is described. Using the methods and processes described herein, multi-layer metal interconnect structures may be fabricated with minimum recess and/or better planarity. In one example, a copper layer is formed over a dielectric structure including recessed areas and non-recessed areas. The copper layer is planarized at a height above the non-recessed regions, for example, through a CMP process and/or an electropolishing process with dummy structures in the dielectric structure. The planarized copper layer is then electropolished to a height below the non-recessed area height to form a recess. The non-recessed regions of the structure are then etched to planarize the copper layer with the non-recessed regions or reduce the recess of the copper layer.

[0074] **Fig. 19A** illustrates an exemplary dual damascene structure after copper layer **1902**, or other suitable conductive layer, has been formed over the structure. The dual damascene structure

may be formed by any suitable method. For example, methods such as chemical vapor deposition (CVD), spin-on techniques, and the like may form the first dielectric layer 1912. The thickness of dietetic layer **1912** can be in the range of approximately 1000 Å to 5000 Å, and preferably 3000 Å. An etch stop layer **1910,** such as silicon nitride or silicon carbide (SiC) layer is deposited above the dielectric layer **1912**. The thickness of etch stop layer **1910** can be in the range of approximately 200 Å to 1000 Å, and preferably 500 Å. In some examples, etch stop layer **1910** may be omitted and the etch timed to stop at the desired level to form the dual damascene structure. A second dielectric layer **1908** is deposited on etch stop layer **1910** by using CVD or spin-on techniques, for example. The thickness of second dielectric layer **1908** can be in the range of approximately 1000 Å to 4000 Å, and preferably 2000 Å. A hard mask layer or a second etch stop layer **1906** is deposited on the second dielectric layer **1908**. The hard mask layer or etch stop layer **1906** may be made of suitable materials such as SiO, SiC, SiN, and the like. The trench and via may be formed by successive formations of photo masks and etches as is known in the art. For example, a first photo mask may be formed for etching the trench followed by a second photo mask to etch the via.

[0075] After etching trench and via, the barrier layer **1904** is deposited by CVD, physical vapor deposition (PVD), or atomic layer deposition. The thickness of barrier layer **1904** can be in the range of 20 Å to 250 Å, depending on trench size and deposition techniques. Barrier layer **1904** may include any suitable material, such as Tantalum (Ta), TaN, Titanium (Ti), TiN, TaSiN, Tungsten (W), WN, WSiN, and the like. After barrier layer **1904** deposition, copper seed layer (not shown on drawing) can be deposited on barrier layer **1904** by CVD, PVD, or ALD. Then copper layer **1902** is deposited on copper seed layer, for example, by CVD, PVD, electroplating, electroless plating techniques, and the like.

[0076] As seen in **Fig. 19A**, copper layer **1902** may include recessed regions **1916r** corresponding to the trench and via areas depending on the particular deposition process. Planarity of copper layer **1902** may be increased by chemical mechanical polishing (CMP) a distance sufficient to remove the recess by including dummy structures within recesses of the dielectric structure for hump free plating techniques and the like. Copper layer **1902** is shown in **Fig. 19B** after a planarization process. An exemplary planarization method using a combination of CMP and electropolishing is described in U.S. application Serial No. 60/313,086, entitled METHODS TO PLANARIZE COPPER DAMASCENE STRUCTURE USING A COMBINATION OF CMP AND ELECTROPOLISHING, filed on August 17, 2001, the entire content of which is incorporated herein by reference.

[0077] Copper layer **1902** is polished from non-recessed regions **1916n** by an electropolishing method to isolate the copper from adjacent trenches and vias (not shown). In one exemplary process, copper layer **1902** is polished to a height δh below the height of etch stop layer **1906** or

non-recessed regions **1916n**. The recess δh allows for a robust electropolishing process and increases the probability that all copper on the non-recessed portions **1916** has been removed. The δh can be in the range of 100 Å to 1500 Å, preferably 500 Å. An exemplary process is described, e.g., in PCT Application No. PCT/US99/15506, entitled METHODS AND APPARATUS FOR ELECTROPOLISHING METAL INTERCONNECTIONS ON SEMICONDUCTOR DEVICES, filed on July 8, 1999, the entire content of which is incorporated herein by reference. The recess of copper layer **1902** will cause poor planarity when another dielectric layer, masking layer, or the like is deposited over the structure. For example, the poor planarity can cause defocus of a lithography process, and the like.

[0078] To reduce the height of non-recessed regions **1916r**, barrier layer **1904** and in some instances a portion of hard mask layer **1906** may be etched away by plasma etching, wet etching, or the like to form a planar top surface of the structure as illustrated in **Fig. 1D**. In one example, a portion of the hard mask layer **1906** is etched such that the surface level or height of copper layer **1902** is planar with the surface of the remaining portion of hard mask layer **1906**.

[0079] Generally, it is desired that the polish of copper layer **1902** result in a δh less than the total thickness of barrier layer **1904** and the thickness of hard mask layer **1906**. If δh is too great, the low dielectric constant k of dielectric layer **1908** will be exposed when barrier layer **1902** is etched away from the nonrecessed regions **1916r** of the structure. This may lead to dielectric layer **1908** being etched, for example, by a plasma etch. Generally, the plasma etch rate of the low k material is higher than that of hard mask **1906** and copper layer **1902**. An etch may also damage or increase the k of dielectric layer **1908** if dielectric layer **1908** is exposed.

[0080] After the etching process, a polymer layer (not shown) may be formed on the surface of copper layer **1902** and hard mask layer **1906**. Typically, the polymer layer is cleaned before additional layers are deposited. The polymer may be cleaned, for example, by a suitable plasma dry ashing process or chemical wet cleaning process.

[0081] A dielectric layer **1926** such as silicon nitride or SiC can be formed on copper layer **1902** and hard mask layer **1906**, as shown in **Fig. 19E**. The thickness of dielectric layer **1926** can be in the range of 200 Å to 1000 Å, and preferably 500 Å. Additionally, a passivation layer or the like may be included over the structure.

[0082] As shown in **Fig. 19F**, the processes described in **Fig. 19A** may be repeated above dielectric layer **1926**. Specifically, additional trenches and vias may be formed with a dielectric layer **1920** and dielectric layer **1924** formed on etch stop layers **1922** and **1926**. Additionally, barrier layer **1916** may be formed over the structure as well as a seed layer (not shown) and copper layer **1914**. A similar process to **Figs. 19B-19E** may be performed to produce a planar structure.

[0083] Figs. 20A-20D illustrate another exemplary method for reducing the recess in a metal trench or metal pad after an electropolishing process. In this instance the structure includes a dielectric layer 2012 patterned with recessed regions 2016r and non-recessed regions 2016n. The non-recessed regions 2016r further include a multi-layer hard mask layer including, for example, a lower hard mask layer 2006 and upper hard mask layer 2007. In one example, the upper hard mask layer 2007 serves as a sacrificial layer to an etching process and the lower hard mask layer 2006 serves as an etch stop layer as described below. Hard mask layers 2007 and 2006 may be made of suitable materials such as SiO, SiC, SiN, and the like. A barrier/seed layer 2004 and metal layer 2002 are deposited over the structure filling the recessed regions 2016r.

[0084] Similar to Figs. 19B and 19C, metal layer 2002 is planarized and electropolished to a height δh below the height of non-recessed regions 2016n as shown in Figs. 20B and 20C. Metal layer is preferably etched to a height substantially planar with lower mask 2006. Barrier layer 2004 and upper hard mask layer 2007 may be selectively etched away to lower mask hard layer 2006, where upper hard mask layer 2007 serves as a sacrificial layer and lower hard mask layer 2006 serves as an etch stop layer. For example, the materials of upper hard mask layer 2007 and lower hard mask layer 2006 may be selected such that a plasma etch or the like removes upper hard mask layer 2007 and stops at lower hard mask layer 2006. The resulting surface of metal layer 2002 and lower hard mask layer 2006 are substantially parallel as illustrated in Fig. 20D.

[0085] Using the methods and processes described herein, multi-layer metal e.g., copper, interconnect structure can be fabricated with minimum recess and/or better planarity. Although the exemplary methods for reducing recesses in copper electropolishing have been described with respect to certain embodiments, examples, and applications, it will be apparent to those skilled in the art that various modifications and changes are contemplated. For example, various dielectric materials and processing techniques to planarize the copper layer, polish the metal layer and the like may be used.

III. Improving Surface Roughness

[0086] In an electropolishing process the surface of the metal layer may be rough causing degradation of the performance of semiconductor devices. For instance, the surface of a copper layer after electropolishing can have a surface roughness of up to a few hundred nanometers. Increased surface roughness may result in poor planarization, surface corrosion, yield loss, and the like. The grain size of a metal layer can be controlled during various stages of exemplary plating and polishing processes to improve device performance and characteristics. In particular, during a plating process, additives such as brightener, leveler, and the like, can be used to control the grain size. Furthermore, the amount of time between the plating process and the electropolishing process

can be shortened to reduce the grain size. In addition, an annealing process can be used to increase grain size after electropolishing to improve electrical characteristics. Electropolishing metal layers and metal interconnections on semiconductor devices is described, e.g., in U.S. Patent Application Serial No. 09/497,894, entitled METHODS AND APPARATUS FOR ELECTROPOLISHING METAL INTERCONNECTIONS ON SEMICONDUCTOR DEVICES, filed on February 4, 2000, which is incorporated in its entirety by reference.

[0087] The amount of surface roughness after electropolishing can depend, at least in part, on the microstructure of the metal layer being electropolished. In particular, **Figs. 21A-21D** illustrate a semiconductor wafer **1000** after an electropolishing process and including metal layers with different microstructures. The metal layers may also be formed within a trench or via of a semiconductor structure or the like. Typically, the size of the grains within the microstructure affect the surface roughness of the metal layer after electropolishing because the removal or polishing rate of the metal layer at the grain boundary and at the grain surfaces may differ. Furthermore, the polishing rate of the metal layer **2102** at different grain faces may differ. Accordingly, as illustrated in **Figs. 21A-21D** and metal layers **2102, 2104, 2106,** and **2108,** having increasingly larger grain sizes, the surface topography after electropolishing can vary based on the size of the grains in the metal layer. Generally, the smaller the grain sizes the lower the surface roughness of the polished metal layer as seen in **Fig. 21A**. Similarly, the larger the grain size, the higher the surface roughness of polished metal layer as seen in **Fig. 21D**.

[0088] **Figs. 22A-22C** show images of a copper layer having a relatively large grain size, e.g., a few microns. In particular, with reference to **Fig. 22A**, a scanning electron microscope (SEM) image of the copper layer surface after electropolishing is shown. With reference to **Fig. 22B**, a focused ion beam (FIB) image of the same copper layer surface after electropolishing is shown from the same location as shown in **Fig. 22A**. The images shown in **Figs. 22A** and **22B** indicate that the surface roughness of the copper layer can have a pattern that matches the pattern of the grains in the copper layer. In addition, **Fig. 22C** shows an atomic force microscope (AFM) image of the copper layer surface after electropolishing. Based on this AFM image, the mean roughness (R_a) of the copper layer surface is 14 nm, and the max height (R_{max}) of the copper layer surface is 113 nm.

[0089] In contrast to **Figs. 22A-22C, Figs. 23A-23C** show images of a copper layer having a relatively small grain size, e.g., tens of nanometers. In particular, with reference to **Fig. 23A**, a scanning electron microscope (SEM) image of the copper layer surface before electropolishing is shown. With reference to **Fig. 23B**, a SEM image of the copper layer surface after electropolishing is shown. The images in **Figs. 23A** and **23B** indicate that if a copper layer surface has a small grain size before electropolishing, the copper layer surface may have a smooth surface after

electropolishing. In addition, **Fig. 23C** shows an atomic force microscope (AFM) image of the copper layer surface after electropolishing. Based on this AFM image, the mean roughness (R_a) of the copper layer surface is 3.6 nm, and the max height (R_{max}) of the copper layer surface is 30 nm.

[0090] **Fig. 24** is a graph showing the relationship between grain size and surface roughness of a copper layer surface after electropolishing for various chemicals included in an electrolyte fluid. Generally, the surface roughness after electropolishing increases as the grain size of the metal layer increases. Thus, a smaller grain size leads to a smoother and more planar copper layer surface topology after electropolishing. Accordingly, controlling and reducing the grain size may reduce the surface roughness of the copper layer, improve planarization, surface corrosion, and yield loss.

[0091] 1.Using additives to control the grain size:

[0092] In one exemplary process for controlling or reducing the metal layer grain size additives may be included in the electrolyte fluid. Additives such as brightener, accelerator, suppressor, leveler, and the like, can be used alone or in combination during the plating process to control the grain structure and enhance the gap filling capability of a metal layer on a semiconductor structure. In particular, additives such as brightener, accelerator, leveler, and the like, can be added to a plating bath to control the grain size and grain structure. For example, a ViaForm plating bath, which is manufactured and commercially available from Enthone-OMI, can be used to obtain a smaller grain size, e.g., as grain size of less than a few hundred Angstroms. The ViaForm plating bath includes an accelerator, suppressor, and leveler. In particular, the accelerator has a concentration in the range of about 1.5 ml/liter to about 2.5 ml/liter, and preferably about 2 ml/liter. The suppressor has a concentration in the range of about 7 ml/liter to about 9 ml/liter, and preferably about 8 ml/liter. The leveler has a concentration in the range of about 1.25 ml/liter to about 1.75 ml/liter, and preferably about 1.5 ml/liter. Although particular concentrations of additives are described above, it should be noted that the concentrations of additives can vary depending on the application. Accordingly, the concentrations of additives can fall outside of the above-described range depending on the particular application and process. The smaller grain size metal layer may then be electropolished with enhanced surface roughness.

[0093] 2.Shortening the time between plating and electropolishing:

[0094] Another exemplary process for controlling or reducing metal layer grain size includes reducing the time between a plating process and an electropolishing process. Typically, after a plating process, the metal layer grain size increases over time. **Figs. 25A-25D** illustrate the change in a metal layer plated on a semiconductor wafer over a period of time. With reference to **Fig. 25A**, after being plated onto wafer **2500**, metal layer **2502** can have a microstructure with a small grain size on the order of a few nanometers. Over time, with reference to **Fig. 25B**, the grains in metal

layer **2502** can grow to a size on the order of tens of nanometers. With reference to **Fig. 25C**, the grains in metal layer **2502** can continue to grow over time to a size on the order of hundreds of nanometers. Finally, with reference to **Fig. 25D**, the grains in metal layer **2502** can grow to a size on the order of a few microns.

[0095] **Fig. 26** is a graph showing the general relationship between the time after plating and the metal layer grain size. Shortly after plating a metal layer onto a semiconductor wafer or structure, the metal layer grain size can increase slowly from point A to B, where the grain size at point A is less than 100 Angstroms and at point B is less than 1000 Angstroms. Between points B and C, the metal layer grain size can increase more rapidly, where the grain size at point C is less than 10,000 Angstroms. Then, between points C and D, the metal layer can reach a saturated stage, in which the metal layer grain size generally increases more slowly if at all.

[0096] In one example, the time between plating and electropolishing the metal layer to form a metal layer with reduced grain size, is less than about 20 hours, and preferably less than about 5 hours. The time is preferably such that the grain size of the metal layer does not reach the micron, and more preferably the sub-micron size or less.

[0097] 3.Annealing after electropolishing:

[0098] Another exemplary process for control of metal layer grain size includes heating or annealing the metal layer after an electropolishing process. A metal layer may be plated, electropolished, and then annealed after the electropolishing process. During annealing, the metal is heated for a period of time to allow grains within the microstructure of the metal layer to form new grains through a process typically called recrystallization. These new grains can have different and relatively larger sizes from the grains in the microstructure before annealing that may increase the electrical characteristics of the metal. Further, in one example, the metal layer may be chemical mechanically polished before the electropolishing process.

[0099] **Fig. 27** is a graph showing the relationship between grain growth rate and annealing temperature for copper plated onto seed layers of different thickness. Note that **Fig. 27** may depict the general relationship between grain size growth rate and annealing temperatures for other metals as well. Generally, the grain growth rate increases as the annealing temperature increases and the thickness of the thin film decreases. A seed layer thickness of less than 1,500Å may be used, and preferably about 100Å. Further, as the annealing temperature increases, the time for recrystallization of the copper microstructure decreases.

[00100] In one exemplary process to enhance surface smoothness, the metal layer is electropolished before annealing. More particularly, the processes before electropolishing can be chosen to form small grain sizes in the metal layer in order to reduce surface roughness and increase

planarity after electropolishing. The metal layer is then electropolished and thereafter the metal layer can be annealed using an appropriate annealing temperature, such as an annealing temperature between 100 °C and 300 °C, and preferably 150 °C, to form larger grain sizes within the metal layer. Alternatively, the metal layer may be annealed over a sufficient time period. These larger grain sizes can improve the electrical properties of the metal layer within vias, plugs, trenches, and the like, of the semiconductor device. Furthermore, if the metal layer is annealed after electropolishing, the surface of the metal layer can remain smooth, while the electrical properties of the metal layer are improved. The metal layer may be heated to annealing temperatures by any suitable method such as an infrared source with a rapid thermal process, an oven, and the like.

[00101] Although the exemplary methods for enhancing surface roughness have been described with respect to certain embodiments, examples, and applications, it will be apparent to those skilled in the art that various modifications and changes are contemplated.

IV. Method for Reducing Non-Uniformity and Recess

[00102] According to one aspect, an exemplary method for reducing non-uniformity and recess in a metal trench or metal pad after an electropolishing process is described. The exemplary method includes applying an alternating forward and reverse voltage pulse that may reduce the build-up of charge and improve copper recess uniformity and reduce the current loading effect.

[00103] **Fig. 28A** illustrates an exemplary electropolishing apparatus, which has been previously disclosed in U.S. Patent No. 6,395,152, entitled METHODS AND APPARATUS FOR ELECTROPOLISHING METAL INTERCONNECTIONS ON SEMICONDUCTOR DEVICES, filed on July 9, 1999, the entire content of which is incorporated herein by reference, and in PCT Application No. PCT/US99/00964, entitled PLATING APPARATUS AND METHOD, filed on January 15, 1999, which is incorporated in its entirety by reference.

[00104] As shown in **Fig. 28A**, wafer **2802** can be rotated around its center axis and may also be translated in the x-axis direction such that electrolyte fluid **2806** from nozzle **2810** can reach any location of the opposing major surface of wafer **2802**. Nozzle **2810** can also be mobile and translate along the x-axis independent of wafer **2802**. The trajectory of electrolyte fluid **2806** on wafer **2802** may be a spiral curve or other suitable trajectory to direct electrolyte fluid **2806** to desired portions of wafer **2802**. Power supply **2812** can operate at a constant current DC, pulse or RF mode or constant voltage DC, pulse or RF mode to provide a potential difference between metal film **2804** and a nozzle electrode **2808** to electropolish a metal film or copper film **2804** on wafer **2802**.

[00105] As shown in **Fig. 28B**, when metal film **2804** on the field of a die **2818** including trenches and/or vias is removed, the copper films on the wafer **2802** will not fully cover wafer **2802**. As

electrolyte fluid **2806** is directed to different portions of wafer **2802**, the copper area within the column of electrolyte fluid **2806** will vary.

[00106] **Figs. 29A** through **29D** show the process of the stream of electrolyte fluid **2906** approaching die **2918** in more detail. If the power supply is running at a constant current, the current density will be low in **Fig. 29A** since the electrolyte column **2906** has not reached die **2918**. During this portion the current is passed primarily through a barrier layer or the like formed on the wafer, which generally has a much lower conductivity than the metal layer.

[00107] As shown in **Fig. 29B**, when electrolyte column **2906** reaches die **2918**, the current density in the portion of the stream of electrolyte fluid **2906** over die **2918** increases to a high value. The current density increases over die **2918** because copper is more conductive and easily polished than typical barrier layer materials such as Ti, TiN, Ta, or TaN. As the stream of electrolyte fluid **2906** moves fully over die **2918** as shown in **Figs. 29C** and **29D** the polishing current density on die **2918** will reduce and reach a substantially constant value as the current is spread over the full cross-sectional area of the stream of electrolyte fluid **2906**.

[00108] **Figs. 30A-30D** illustrate a cross-sectional view of the exemplary process. As shown in **Fig. 30A**, negative charge (electron) **3080** is built up on the interface between electrolyte fluid **3006** and barrier layer **3005** because barrier layer **3005** is difficult to polish. When electrolyte fluid **3006** is adjacent copper trench **3020**, the negative charge **3080** buildup on the surface of the electrolyte is discharged through trench **3020** thereby increasing the polishing rate of trench **3020**, as shown in **Fig. 30B**.

[00109] With reference to **Figs. 30C** and **30D**, as electrolyte fluid **3006** continues to move over the second trench **3022**, the negative surface charge **3080** is reduced further, causing the polishing rate on trench **3024** to be lower than that on trench **3022**, and the polishing rate on trench **3022** is lower than that on trench **3020** and so on. Due to the changes in current density, the polishing rate will also change accordingly. With reference to **Fig. 30E**, because of the changes in polishing rate the copper recess of the first trench **3020** is larger than that of the second trench **3022**, and the copper recess on the second trench **3022** is larger than that of the third trench **3024** and so on. The copper recess may cause conductance fluctuations of the copper line and degrade the performance of the final device.

[00110] In one aspect, an exemplary electropolishing method is described using pulse or alternating current voltages to minimize the polishing rate differences over trenches and reduce or prevent copper recess. In one example, the relationship of polishing rate uniformity on trenches, pulse frequency, and nozzle tangential moving speed are varied to reduce copper recess in an electropolishing method.

[00111] **Fig. 31** shows an exemplary forward and reverse pulse waveform for an electropolishing method. The waveform region of A to B is the forward pulse, and waveform region of C to D is the reverse pulse. V_1 is the forward pulse voltage and V_2 is the reverse pulse voltage. t_0 is the pulse period, typically the time passed from A to E. The forward pulse width is t_1 and the reverse pulse width is t_2. The duty cycle in percentage is t_1/t_0.

[00112] **Figs. 32A - Fig. 32F** illustrate an exemplary electropolishing method including the pulse waveform of **Fig. 31**. **Fig. 32A** shows electrolyte fluid **3206** approaching trench **3220** and as the pulse waveform is at point "A," and voltage V_1. As illustrated, the interface between electrolyte fluid **3206** and the surface of the wafer is filled with negative charge **3280**.

[00113] **Fig. 32B** illustrates the electrolyte fluid **3206** that has moved a distance L_1 to a location adjacent trench **3220**, and pulse waveform is at point "B." At this edge the pulse waveform moves to point "C," i.e. the reverse pulse region and voltage V_2. The electrolyte interface at point C is charged by positive charge (ions) **3282**, as shown in **Fig. 32C**. In this manner charge of electrolyte fluid **3206** is alternated at the interface between the relatively high conductive metal or copper layer in trench **3220** and the relatively low conductivity barrier layer **3205**.

[00114] As shown in **Fig. 32D**, as the electrolyte fluid **3206** moves a distance L_2 across trench **3220** and pulse waveform moves to point "D," V_2 prevents a high rate of polishing. When electrolyte fluid **3206** has moved partially over first copper trench **3220** the waveform moves to point to point "E," and V_1 to polish copper in trench **3220**. At this time, negative charge **3280** is building up on the interface between electrolyte **3206** and barrier layer **3205**.

[00115] **Fig. 32F** shows that as the pulse waveform moves to point "F," and the stream of electrolyte moves distance L_3, the negative charge **3280** buildup on the interface of barrier and electrolyte will be discharged on the copper in trench **3220**, which may cause a higher polishing rate. The over polishing region width **w**, as shown in **Fig. 32G**, is proportional to the forward pulse width and to the nozzle moving speed, i.e.,

$$\mathbf{w = c\ V\ t_1} \qquad \textbf{(1)}$$

Where **c** is constant, **V** is the tangential speed or velocity of nozzle relative to wafer surface, and $\mathbf{t_1}$ is the forward pulse width (see **Fig. 31**).

[00116] Generally, a smaller **w** will reduce the recess depth **d**. In order to reduce **w**, a lower velocity **V** and a short forward pulse width $\mathbf{t_1}$ are preferred. In order to have a short forward pulse width, exemplary methods may include either reducing the duty cycle ($\mathbf{t_1/t_0}$) or increasing pulse frequency. For example, the duty cycle can be in the range of 20% to 80%, preferably 50%. The

frequency can be in the range of 100 kHz to 100 MHz, preferably 3 MHz. Velocity can be in the range of 100 mm/sec to 2000 mm/sec, preferably 500 mm/sec.

[00117] For example, by substituting $V = 500$ mm/sec, and duty cycle = 50%, and $t_1 = 0.2$ E-6 second (2.5 MHz) into equation (1), then

$$w = c \times 500 \times 0.2E\text{-}6 = c \times 0.1 \times 10^{-6} \text{ mm} = c \times 0.1 \text{ micron}$$

Where w is in the 0.1-micron magnitude range.

[00118] As previously disclosed in provisional application U.S. Serial No. 60/092,316, a variety of pulse or alternative current/power supplies can be used in the exemplary methods, such as a RF power supply, triangle wave power supply, or any other type of power supply which can charge the interface between electrolyte **1008** and barrier to positive and negative side.

[00119] Although the exemplary method for reducing non-uniformity and reducing recess has been described with respect to certain embodiments, examples, and applications, it will be apparent to those skilled in the art that various modifications and changes may be made without departing from the invention.

[00120] The above detailed description is provided to illustrate exemplary embodiments and is not intended to be limiting. It will be apparent to those skilled in the art that numerous modifications and variations within the scope of the present invention are possible. For example, the various processes may be used alone or in combination to improve device manufacturing and performance. Accordingly, the present invention is defined by the appended claims and should not be limited by the description herein.

CLAIMS

1. A method for electroplating a metal layer on a semiconductor structure having recessed regions and non-recessed regions, comprising:

electroplating within a first current density range before the metal layer is planar above recessed regions of a first density; and

electroplating within a second current density range after the metal layer is planar above the recessed regions, wherein the second current range is greater than the first current range.

2. The method of claim 1, wherein the first current density range is between 0.5 mÅ/cm^2 and 5 mÅ/cm^2, and the second current density range is between 5 mÅ/cm^2 and 30 mÅ/cm^2.

3. The method of claim 1, wherein electroplating within the first current density range is carried out at a constant current density.

4. The method of claim 1, wherein electroplating within the first current density range is carried out at an increasing current density.

5. The method of claim 4, wherein the first current density increases linearly.

6. The method of claim 4, wherein the first current density increases non-linearly.

7. The method of claim 1, wherein electroplating within the first current density range includes decreasing the current density.

8. The method of claim 1, wherein electroplating within the second current density range is carried out at a constant current density.

9. The method of claim 1, wherein electroplating within the second current density range is carried out at an increasing current density.

10. The method of claim 9, wherein the second current density increases non-linearly.

11. The method of claim 1, wherein electroplating within the second current density range is carried out at a decreasing current density.

12. The method of claim 1, wherein the recessed regions of a first density include recesses with a size between 0.035 to 0.5 microns and spacing in the range of 0.035 to 0.5 microns, and

a large recess with a dummy structure having a size between 0.05 and 2.0 microns and spacing in the range 0.05 and 2.0 microns.

13. The method of claim 12, wherein the metal layer is electroplated above the regions of the first density until the metal layer is planar above the regions of the first density, and

electroplating over a region of second density until the metal layer is planar above the region of first density and the region of second density, wherein the region of second density is greater than the region of first density.

14. The method of claim 13, wherein after the metal layer is planar above the region of second density and the region of first density, electroplating at a third current density greater than the second current density.

15. The method of claim 1, wherein the metal layer is electroplated with an electrolyte fluid including an accelerator, suppressor, and leveler.

16. The method of claim 15, wherein the accelerator concentration is between 1.5 and 2.5 ml/liter, the suppressor concentration is between 7 and 9 ml/liter, and the leveler concentration is between 1.25 and 1.75 ml/liter.

17. The method of claim 1, further including controlling the grain size of the metal layer with additives in the electrolyte fluid.

18. The method of claim 17, wherein the additives include at least one of a brightener, accelerator, suppressor, and leveler

19. The method of claim 1, further including rotating the semiconductor structure with a chuck at a rotation speed of 50-200 rpm.

20. The method of claim 1, further including rotating the semiconductor structure with a chuck at a rotation speed of 125 rpm.

21. A method for electropolishing a metal layer on a semiconductor structure, comprising:

electropolishing a metal layer formed over recessed regions and non-recessed regions, wherein the metal layer is electropolished to a height less than the height of the non-recessed regions, and the non-recessed regions include a hard mask layer; and

removing at least a portion of the hard mask layer such that the height of the metal layer and the non-recessed regions are substantially planar.

22. The method of claim 21, wherein only a portion of the hard mask layer is removed.

23. The method of claim 21, wherein the hard mask layer is formed over a dielectric layer.

24. The method of claim 21, wherein the hard mask layer includes a sacrificial layer and an etch stop layer.

25. The method of claim 24, wherein the metal layer is electropolished to a height substantially planar with the etch stop layer included in the mask layer.

26. The method of claim 25, wherein the sacrificial layer is removed with an etch having a higher selectivity for the sacrificial layer than the etch stop layer included in the hard mask layer.

27. The method of claim 21, further including planarizing the metal layer formed over the semiconductor structure prior to electropolishing.

28. The method of claim 27, wherein the metal layer is planarized by a chemical mechanical polishing process.

29. The method of claim 21, wherein the semiconductor structure includes dummy structures formed in the recessed regions to increase the planarity of the formed metal layer.

30. The method of claim 21, wherein the non-recessed regions are etched.

31. The method of claim 21, wherein the height of the metal layer is electropolished to a height between 200 Å and 1000 Å less than the height of the non-recessed regions of the structure.

32. The method of claim 21, wherein the height of the metal layer is electropolished to a height of 500 Å less than the height of the non-recessed regions of the structure.

33. The method of claim 21, wherein the non-recessed regions of the structure removed include a barrier layer and an etch stop layer.

34. The method of claim 21, wherein a dielectric layer included in the non-recessed regions of the structure is not etched when etching.

35. The method of claim 21, further including depositing a polymer layer over the metal layer and the non-recessed regions of the structure.

36. The method of claim 21, further including depositing a dielectric layer over the metal layer and the non-recessed regions of the structure.

37. The method of claim 36, further including forming a second semiconductor structure including recessed regions and non-recessed regions over the dielectric layer.

38. A method for forming a metal layer on a semiconductor structure, comprising:
electroplating a metal layer on a semiconductor structure with an electrolyte fluid;
introducing additives to control a grain size of the metal layer in the electrolyte fluid; and
electropolishing the metal layer before such time that the grain size increases to one micron.

39. The method of claim 38, wherein the metal layer is plated with a grain size of less than 200 Å.

40. The method of claim 38, wherein the additive includes a brightener.

41. The method of claim 38, wherein the additive includes an accelerator.

42. The method of claim 41, wherein the accelerator is between 1.5 ml/liter and 2.5 ml/liter.

43. The method of claim 38, wherein the additive includes a suppressor.

44. The method of claim 43, wherein the suppressor is between 7 ml/liter and 9 ml/liter.

45. The method of claim 38, wherein the additive includes a leveler.

46. The method of claim 45, wherein the leveler is between 1.25 ml/liter and 1.75 ml/liter.

47. The method of claim 38, wherein the additive includes at least one of a brightener, accelerator, suppressor, and a leveler.

48. The method of claim 38, further including electropolishing the metal layer, wherein a time between electroplating and electropolishing the metal layer is determined to further control the grain size of the metal layer.

49. The method of claim 38, further including electropolishing the metal layer within 20 hours of electroplating.

50. The method of claim 38, further including electropolishing the metal layer within 5 hours of electroplating.

51. A method for forming a metal layer on a semiconductor structure, comprising:

electroplating a metal layer on a semiconductor structure;

electropolishing the metal layer on the semiconductor structure after electroplating the metal layer; and

annealing the metal layer after it has been electropolished, wherein the annealing increases a grain size of the metal layer.

52. The method of claim 51, further including chemical mechanical polishing the metal layer after electroplating and before electropolishing the metal layer.

53. The method of claim 52, wherein the chemical mechanical polishing planarizes the metal layer.

54. The method of claim 51, wherein the metal layer includes copper.

55. The method of claim 51, wherein the metal layer is plated on a metal seed layer less than 1500 Å in thickness.

56. The method of claim 51, wherein the metal layer is plated on a 100 Å thick metal seed layer.

57. The method of claim 51, wherein the annealing includes heating the metal layer with an infrared source.

58. The method of claim 51, wherein the annealing includes heating the metal layer with an oven

59. The method of claim 51, wherein the annealing includes heating the metal layer between 100 °C and 300 °C.

60. The method of claim 51, wherein the annealing includes heating the metal layer at approximately 150 °C.

61. The method of claim 51, wherein a time between electroplating and electropolishing is determined to control the grain size of the metal layer.

62. The method of claim 61, wherein the time is less than 20 hours.

63. The method of claim 61, wherein the time is less than 5 hours.

64. The method of claim 61, wherein the time is determined to have a grain size of less than 100Å when electropolishing.

65. The method of claim 61, wherein the time is determined to have a grain size of less than 500Å when electropolishing.

66. The method of claim 61, wherein the time is determined to have a grain size of less than 1000Å when electropolishing.

67. A method for electropolishing a metal layer on a semiconductor wafer, comprising:

directing a stream of electrolyte fluid to a metal layer on a semiconductor wafer;

moving the stream of electrolyte fluid and the wafer relative to each other; and

applying an alternating forward and reverse voltage between the nozzle and the metal layer, wherein

a first transition is made between the forward and reverse voltage when the stream of electrolyte fluid is adjacent an interface between the metal layer of a first conductivity and a material of second conductivity, and

the first conductivity is different than the second conductivity.

68. The method of claim 67, further including a second transition between the forward and reverse voltage when the stream of electrolyte fluid is over the metal layer.

69. The method of claim 68, wherein the first transition and second transition reduce overpolishing of the metal layer.

70. The method of claim 67, wherein the material of second conductivity is a barrier layer.

71. The method of claim 67, wherein the metal layer includes copper and the material of second conductivity is a barrier layer.

72. The method of claim 67, wherein the first conductivity is greater than the second conductivity.

73. The method of claim 67, wherein the alternating forward and reverse voltage is pulsed at a frequency in the range of 100 kHz and 100 MHz.

74. The method of claim 67, wherein the alternating forward and reverse voltage is pulsed at a frequency of approximately 3 MHz.

75. The method of claim 67, wherein the forward voltage pulse duration is between a range of 20 and 80 percent of the reverse voltage pulse.

76. The method of claim 67, wherein the forward voltage pulse duration is approximately 50 percent of the reverse voltage pulse.

77. The method of claim 67, wherein the relative velocity of the wafer and the stream of electrolyte fluid is between 100 mm/sec and 2,000 mm/sec.

78. The method of claim 67, wherein the relative velocity of the wafer and the stream of electrolyte fluid is approximately 500 mm/sec.

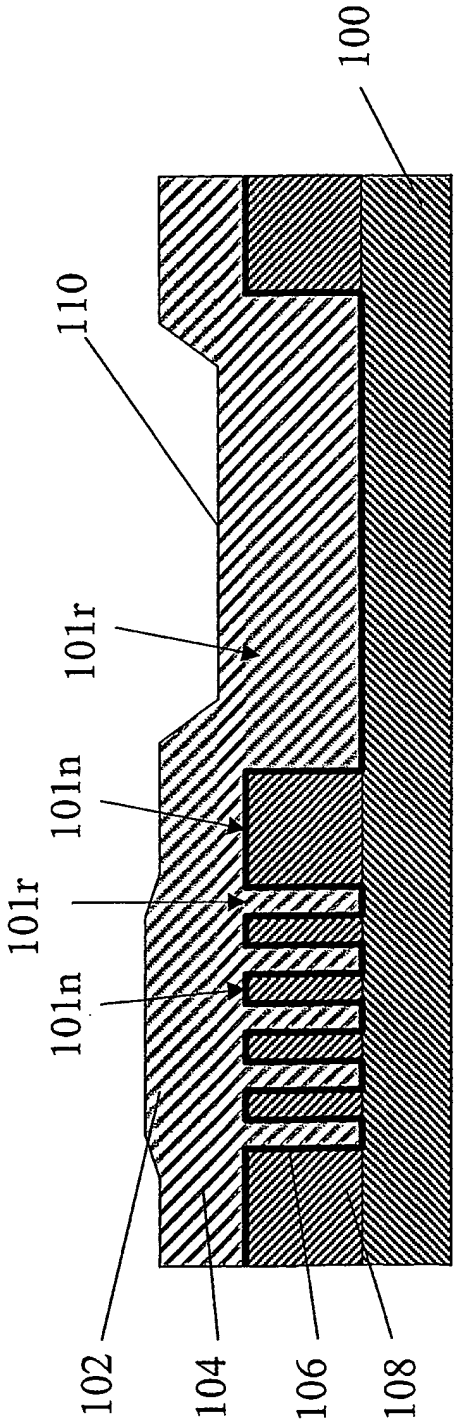

100
110
101r
101n
101r
101n
102
104
106
108

Fig. 1A

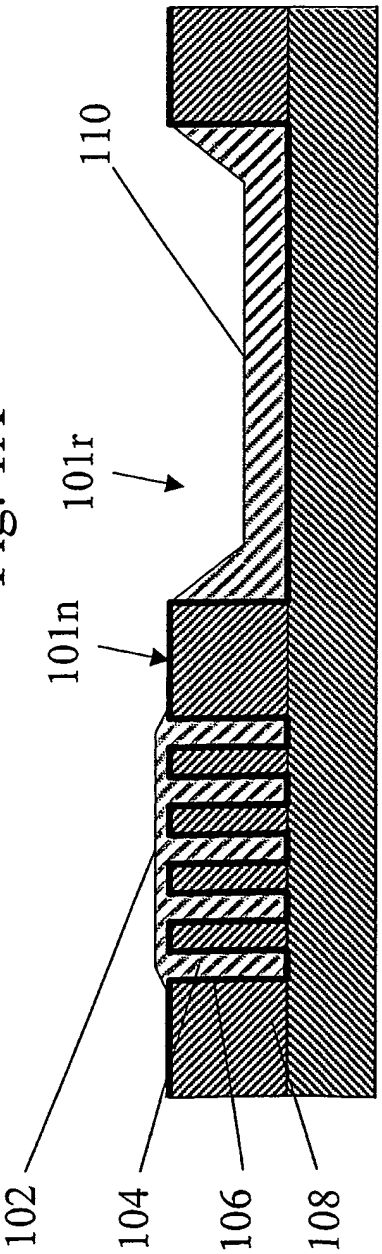
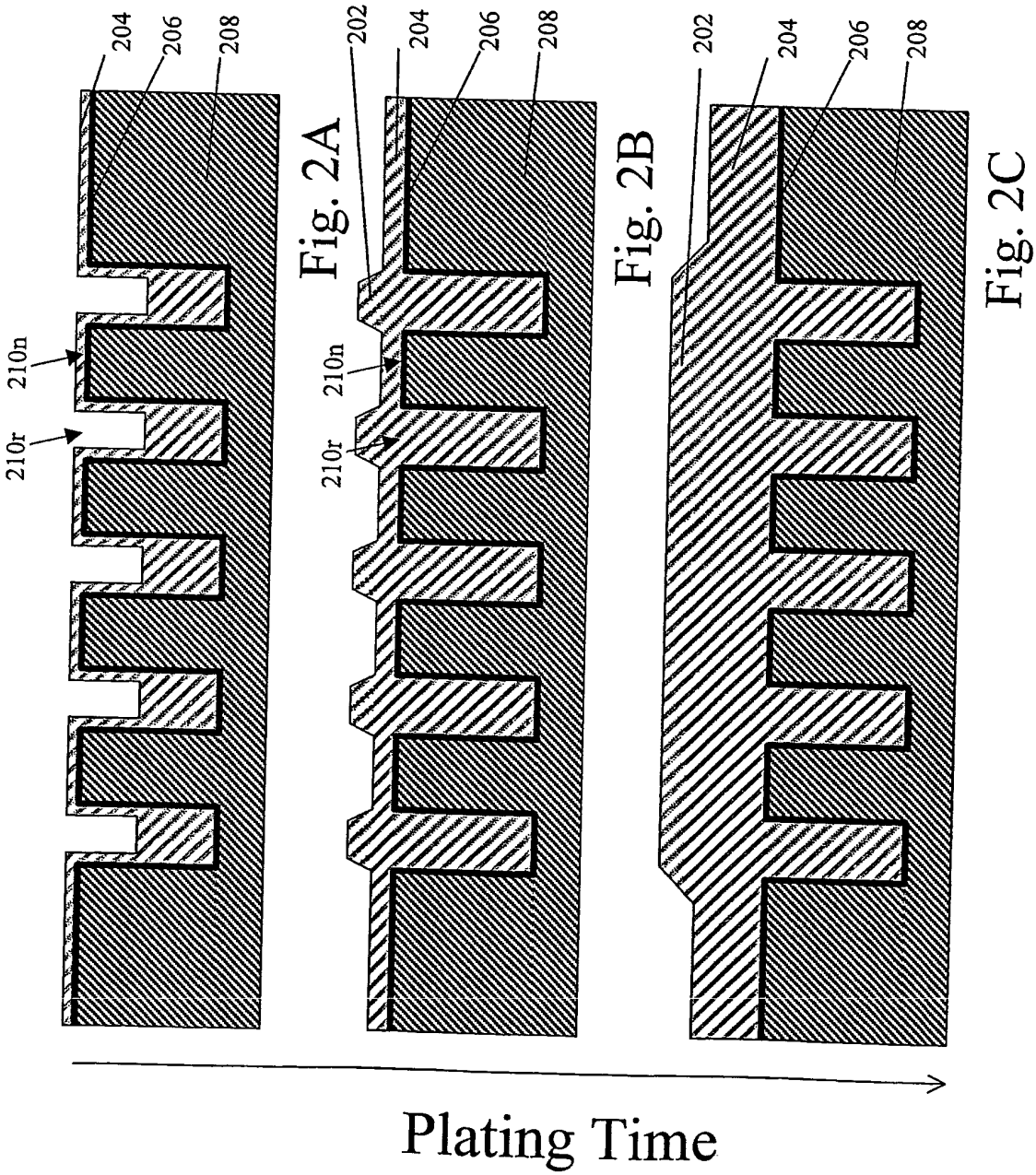

110
101r
101n
102
104
106
108

Fig. 1B


204
206
208
210n
210r
Fig. 2A
202
204
206
208
210n
210r
Fig. 2B
202
204
206
208
Fig. 2C
Plating Time

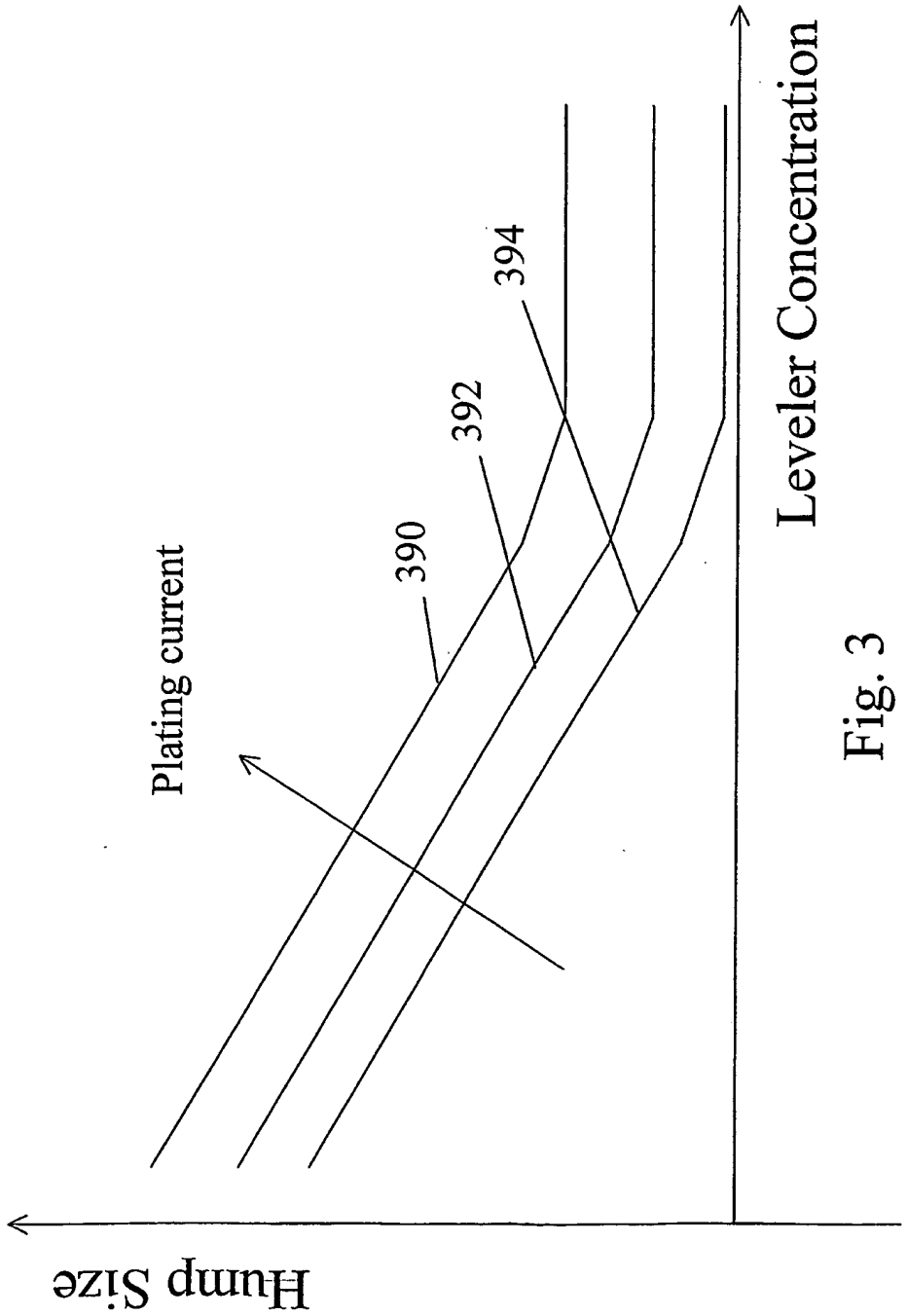

Hump Size
Plating current
390
392
394
Leveler Concentration

Fig. 3

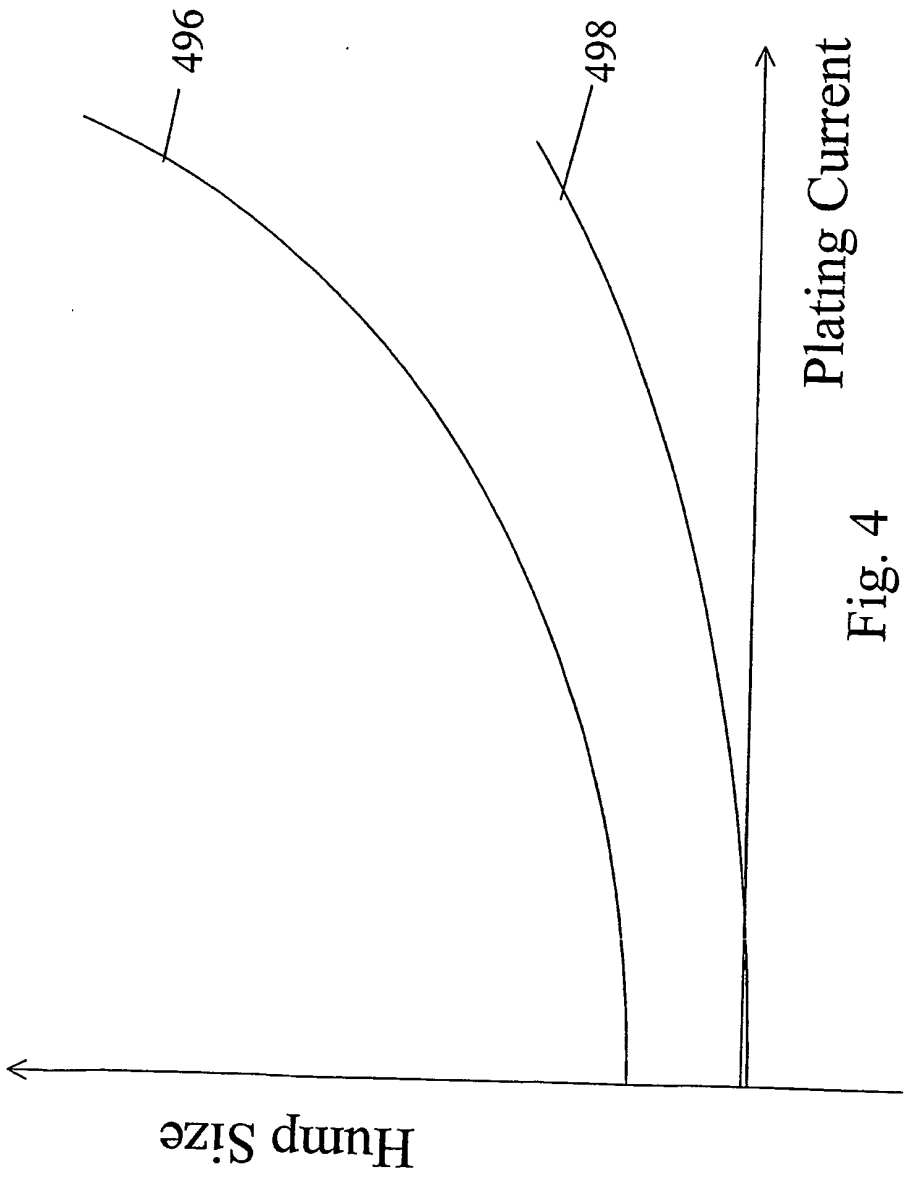


Fig. 4

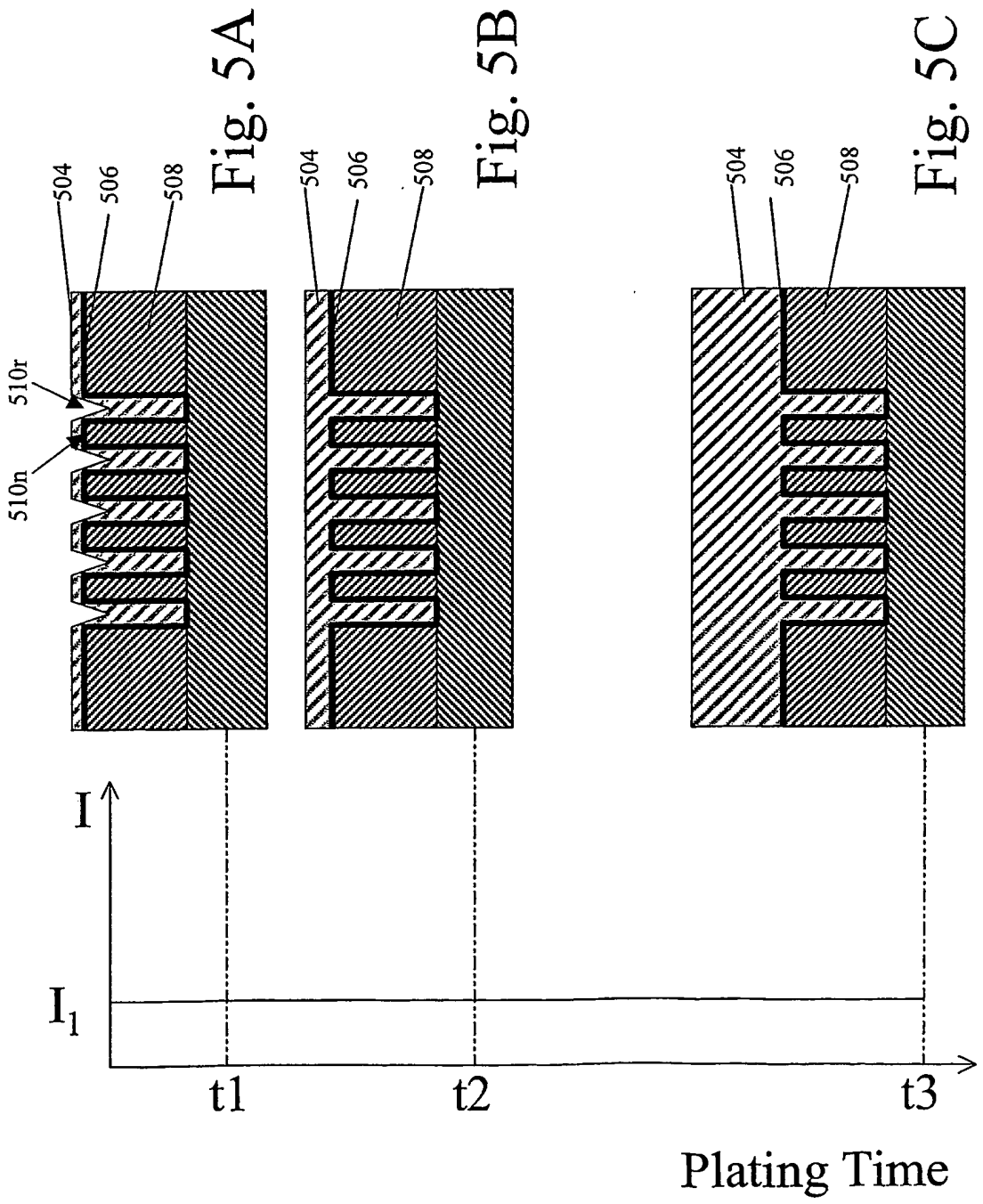


Fig. 5A
Fig. 5B
Fig. 5C
504
506
508
510r
510n
I
I_1
t1
t2
t3
Plating Time

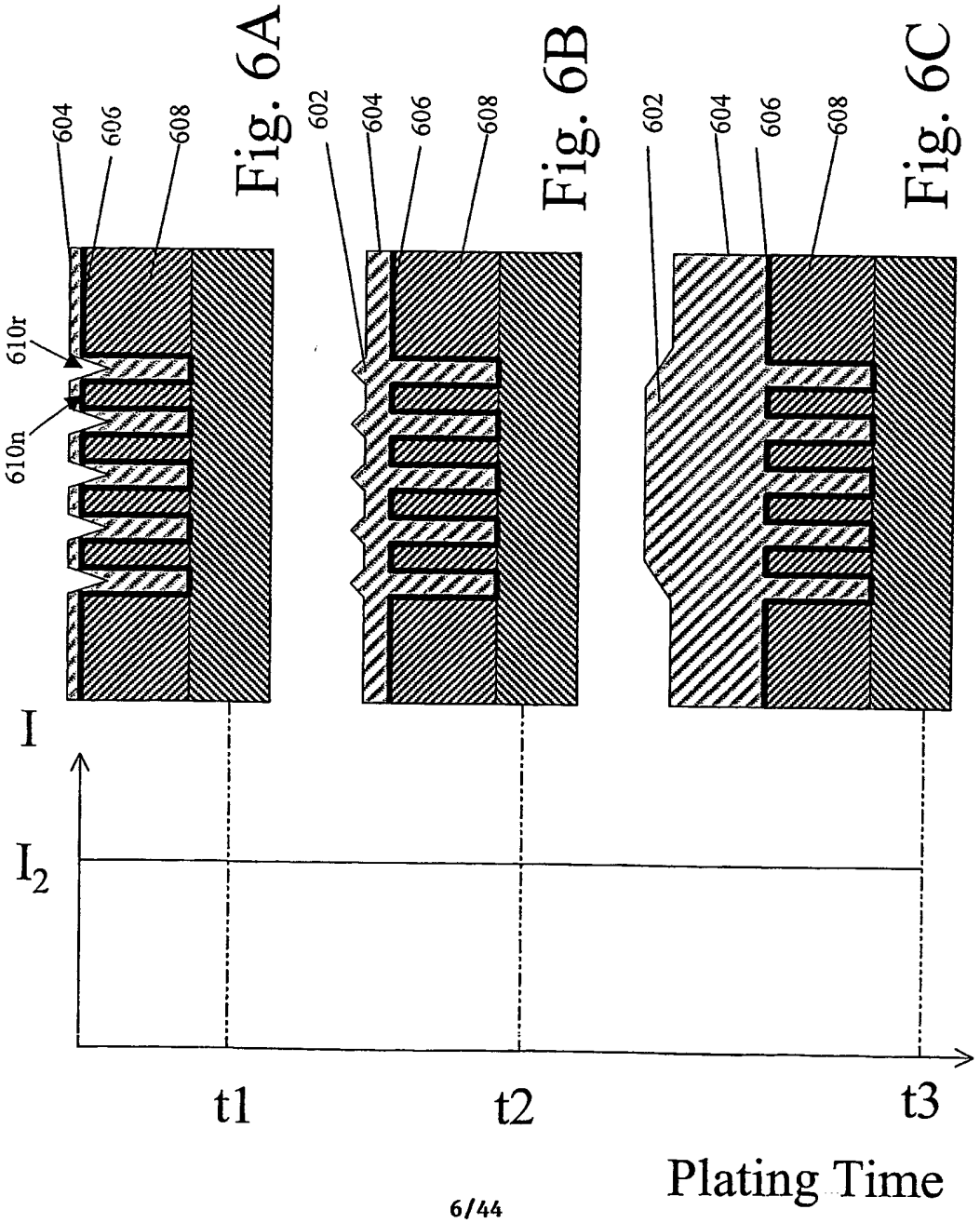


Fig. 6A
Fig. 6B
Fig. 6C
602
604
606
608
610r
610n
I
I_2
t1
t2
t3
Plating Time

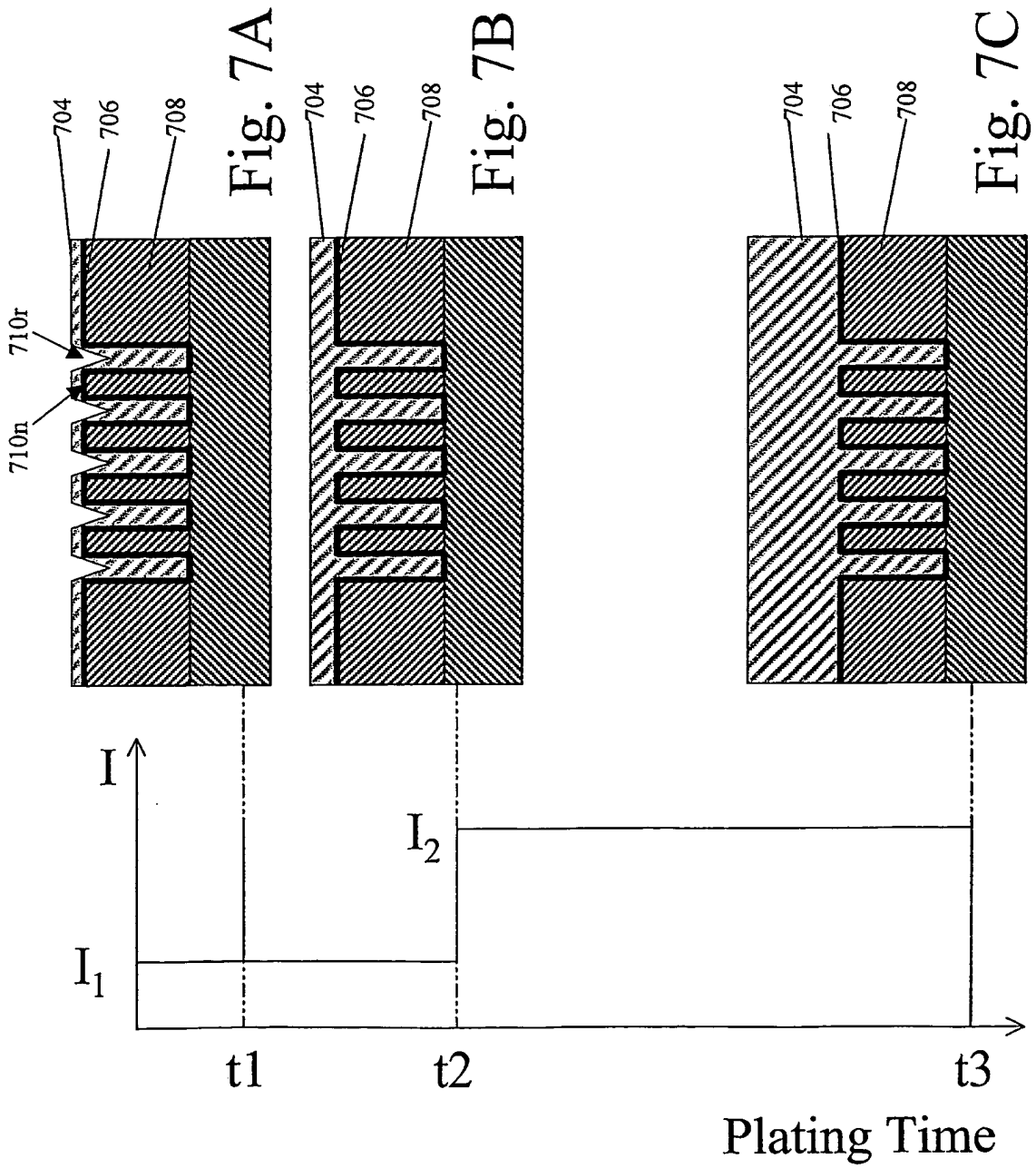


Fig. 7A

Fig. 7B

Fig. 7C

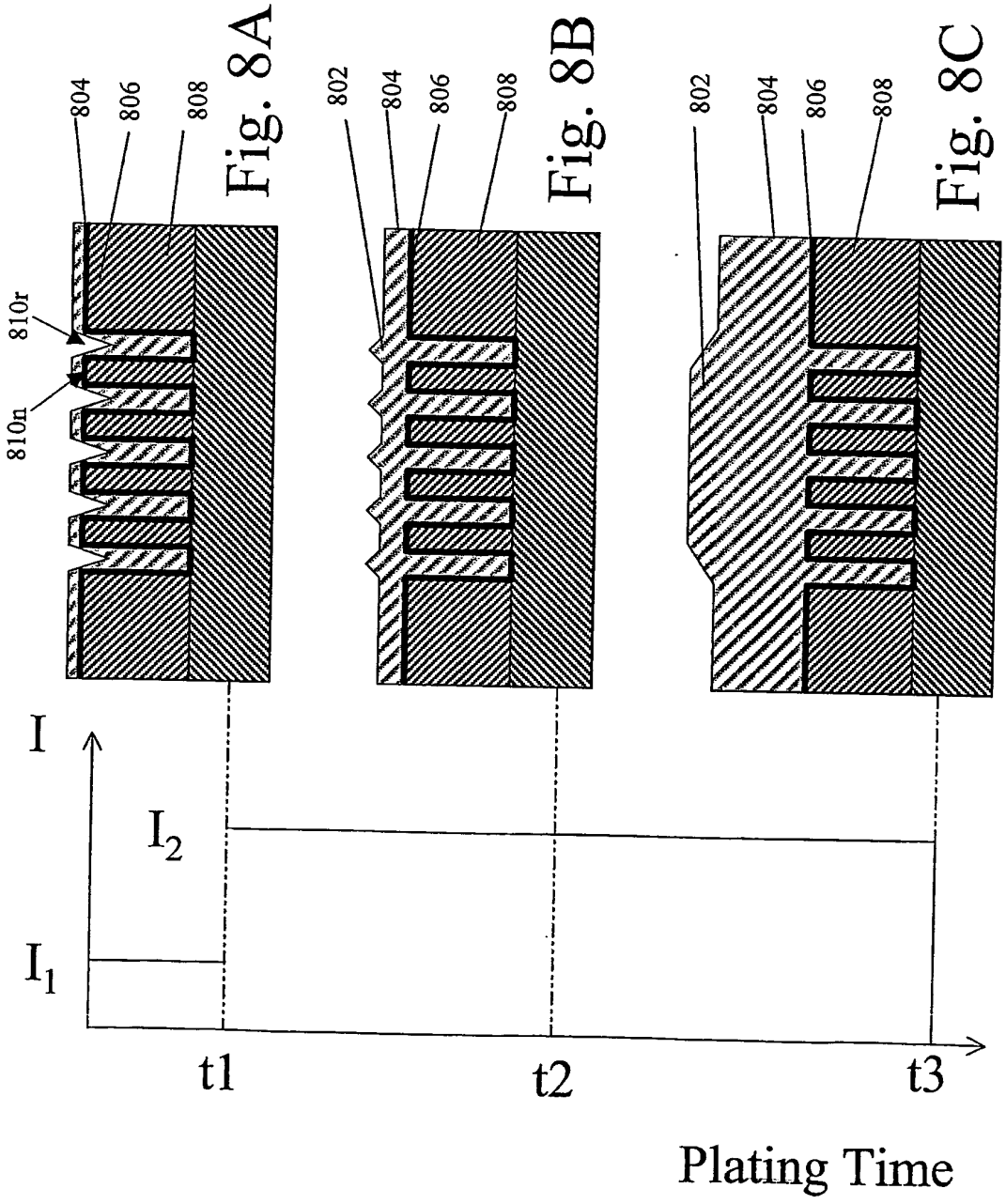


Fig. 8A

Fig. 8B

Fig. 8C

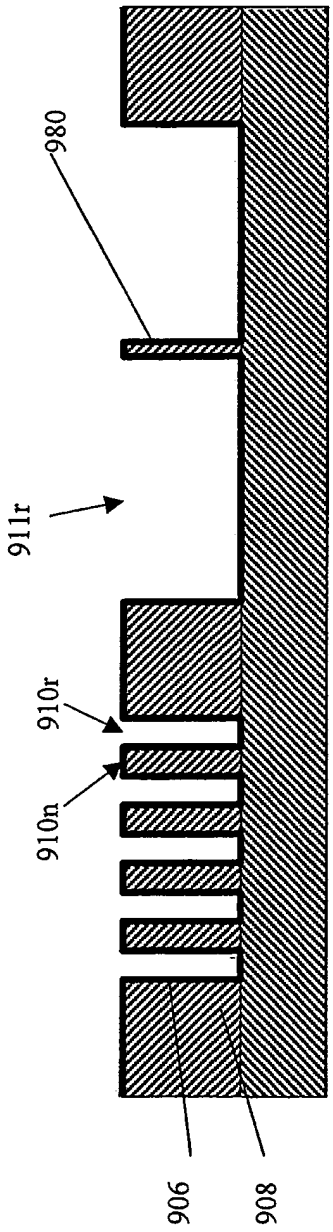


Fig. 9

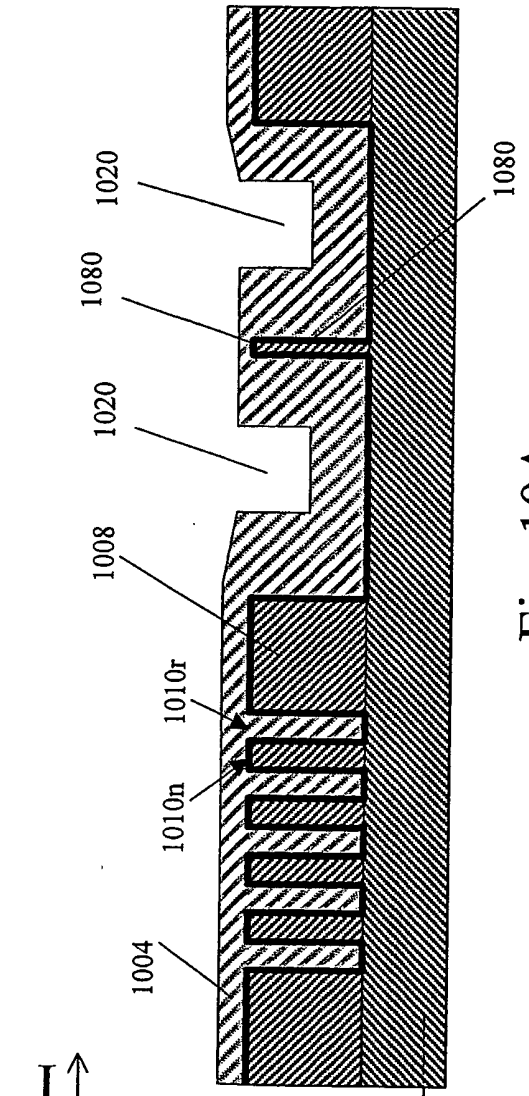


Fig. 10A

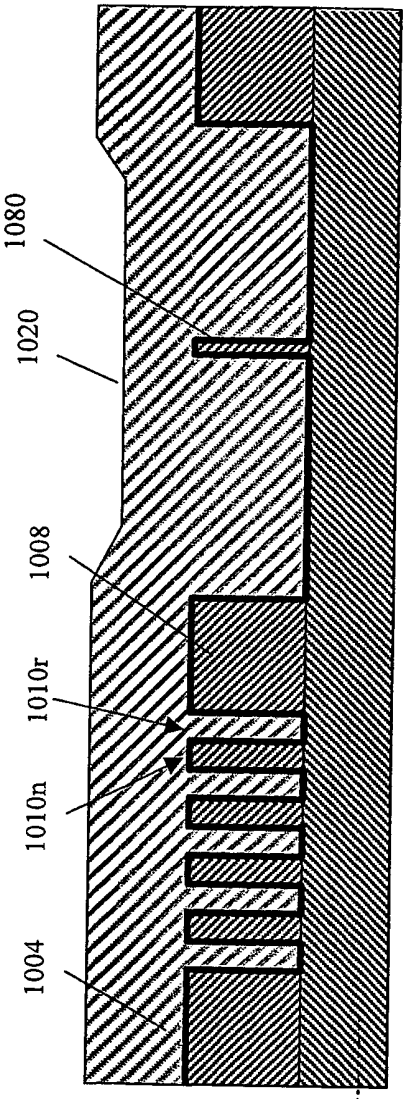
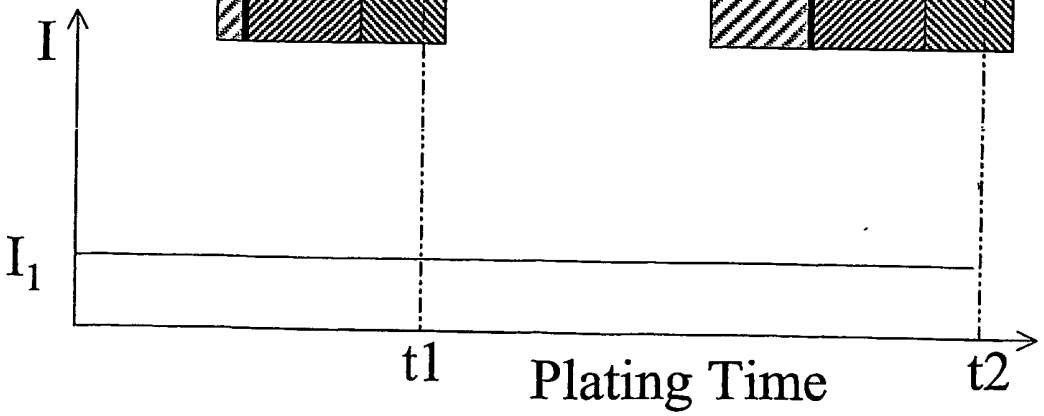


Fig. 10B



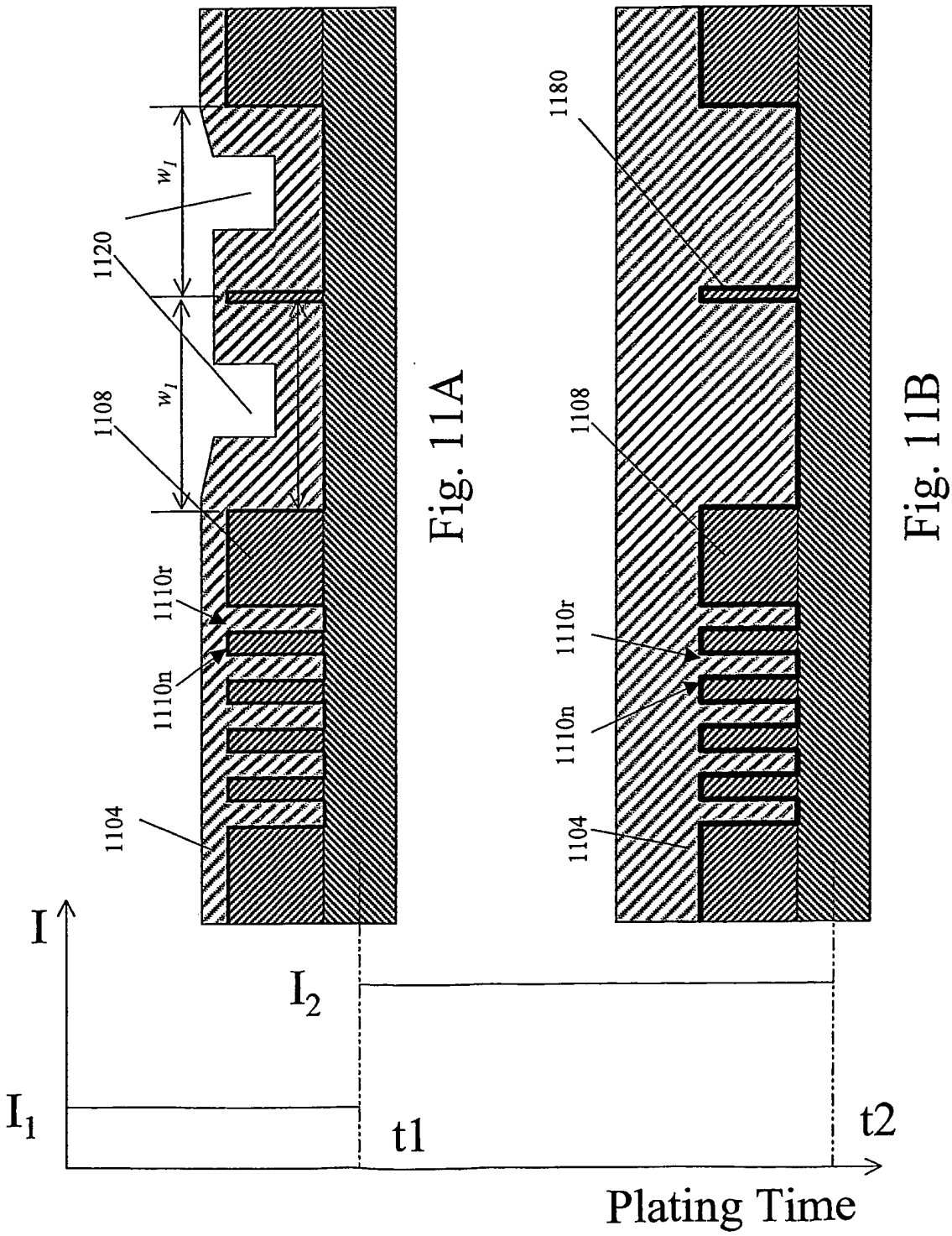


Fig. 11A

Fig. 11B

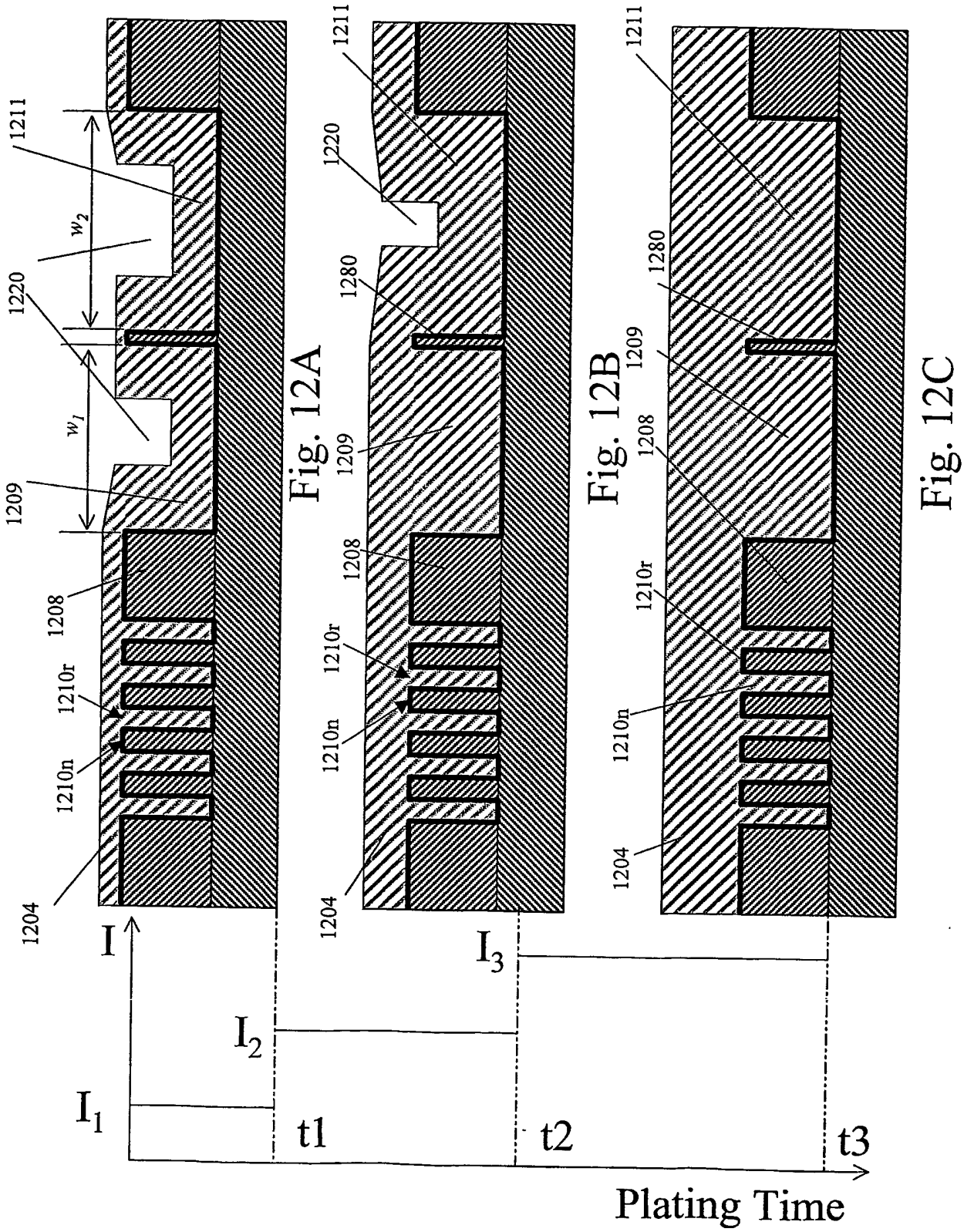


Fig. 12A

Fig. 12B

Fig. 12C

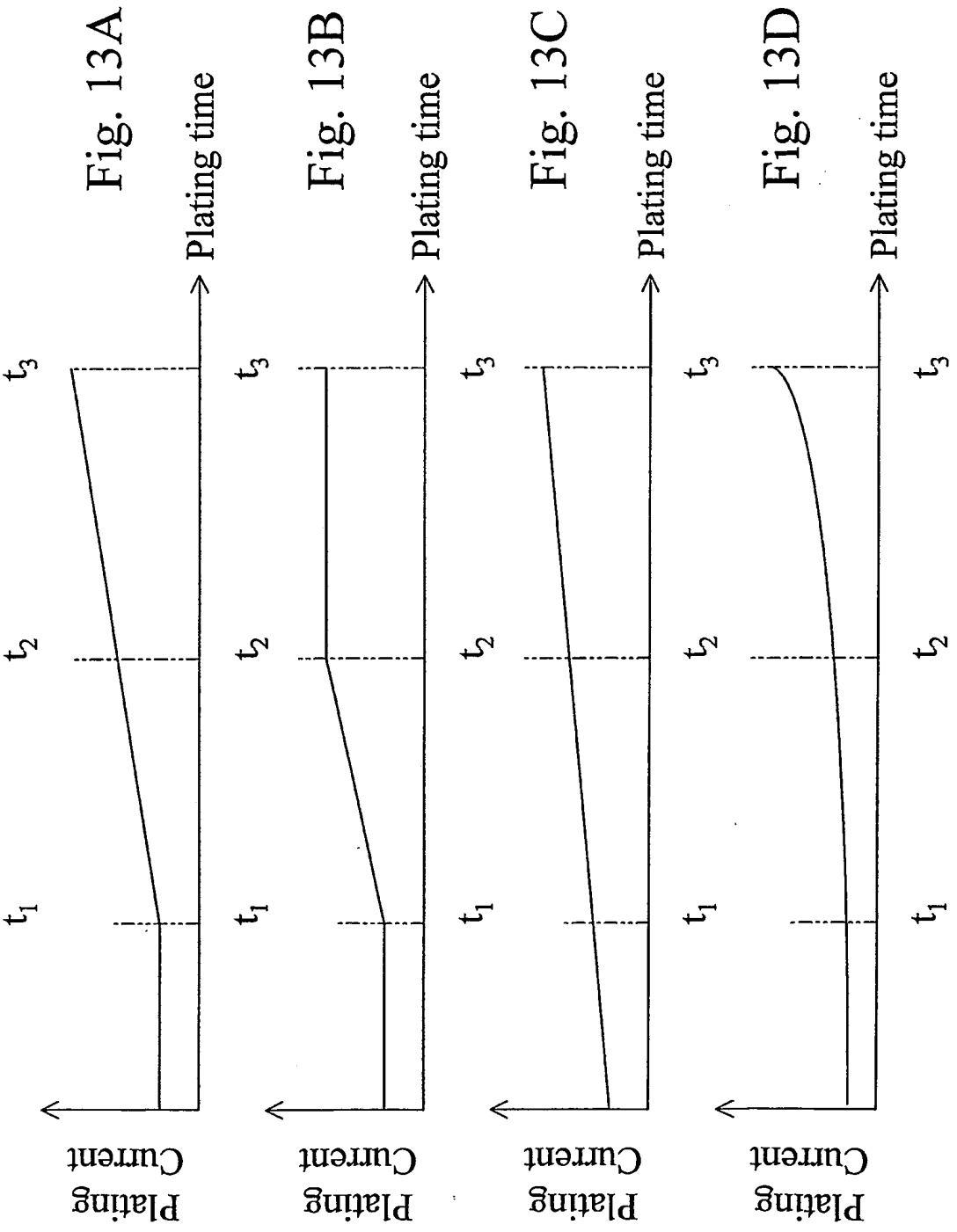


Fig. 13A
Plating Current
Plating time
t_1
t_2
t_3
Fig. 13B
Plating Current
Plating time
t_1
t_2
t_3
Fig. 13C
Plating Current
Plating time
t_1
t_2
t_3
Fig. 13D
Plating Current
Plating time
t_1
t_2
t_3

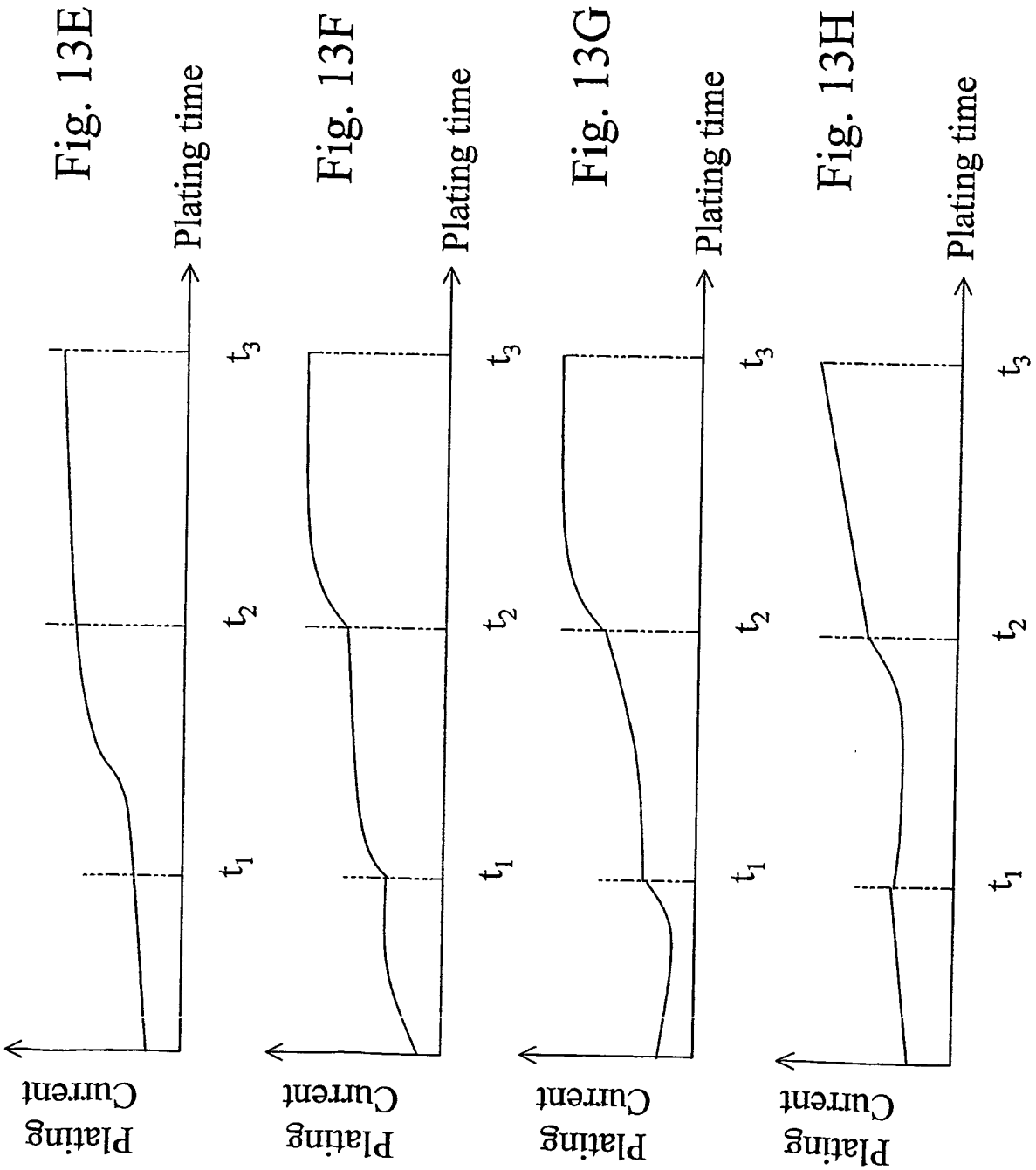


Fig. 13E
Plating time
Plating Current
t_1
t_2
t_3
Fig. 13F
Plating time
Plating Current
t_1
t_2
t_3
Fig. 13G
Plating time
Plating Current
t_1
t_2
t_3
Fig. 13H
Plating time
Plating Current
t_1
t_2
t_3

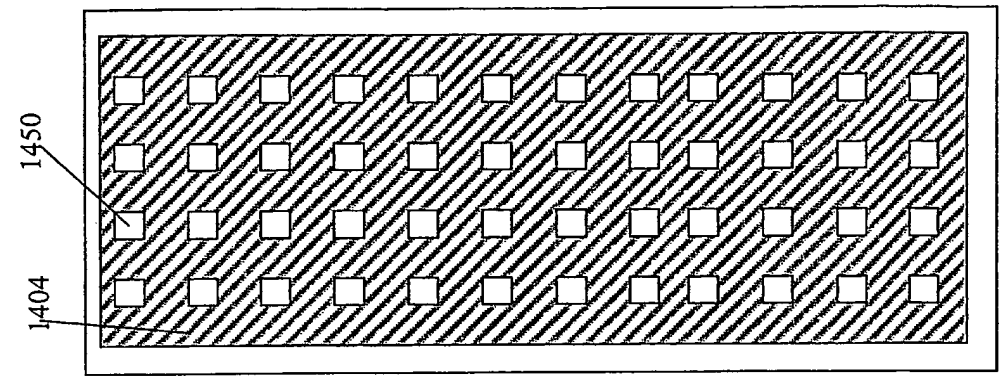


Fig. 14C

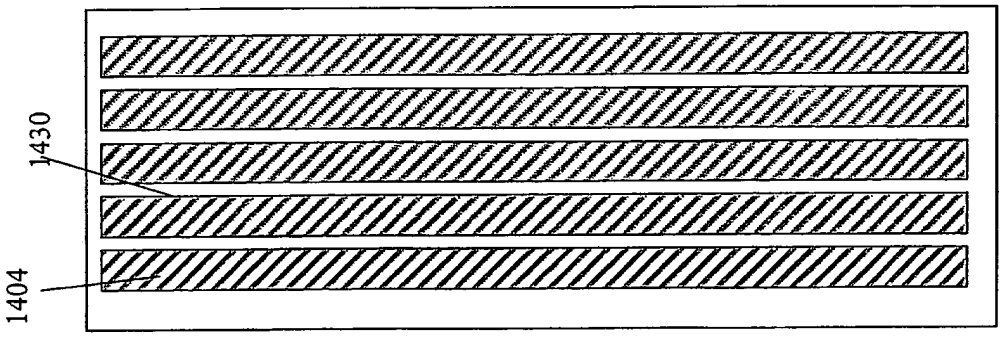


Fig. 14B

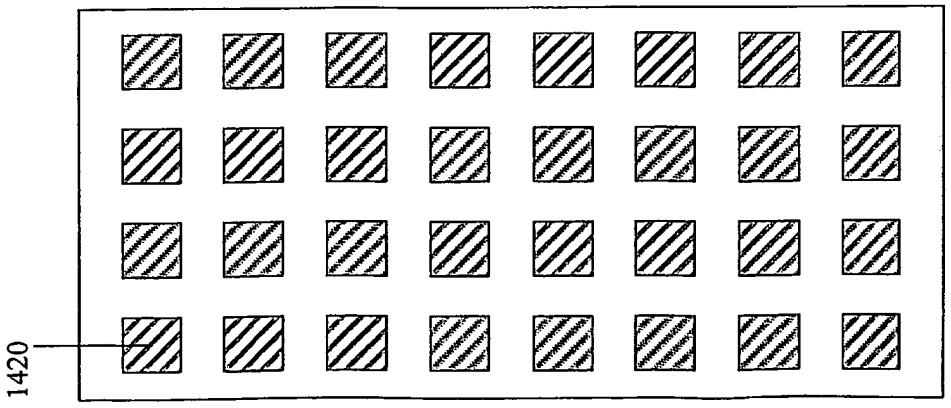


Fig. 14A

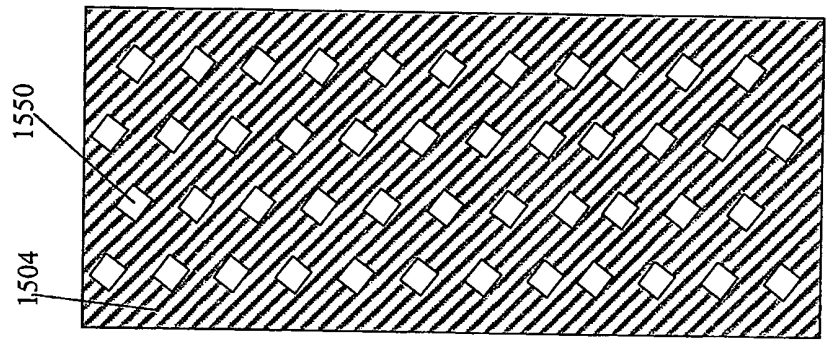


Fig. 15C

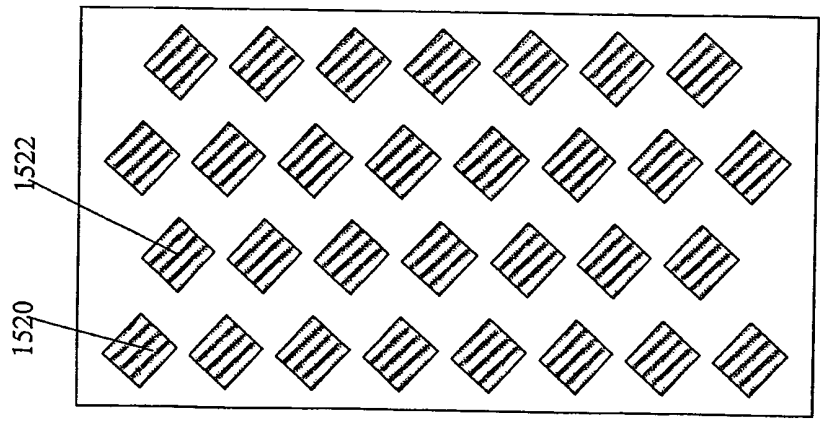


Fig. 15B

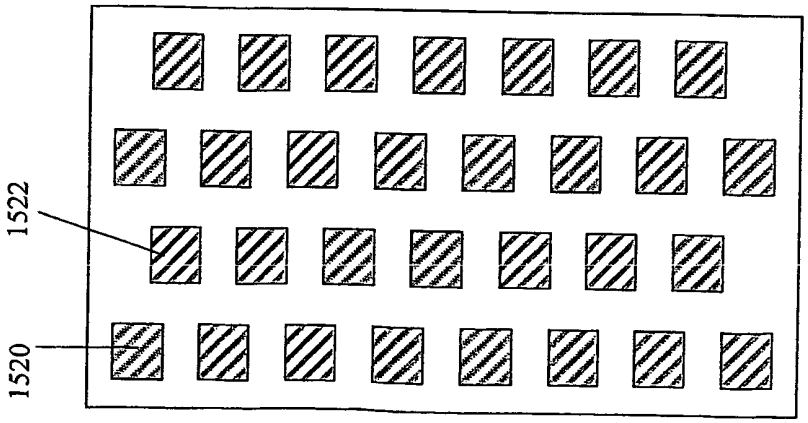


Fig. 15A

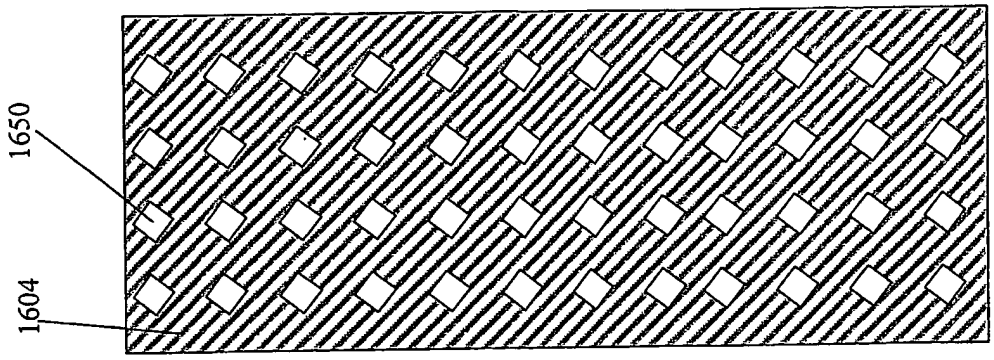


Fig. 16C

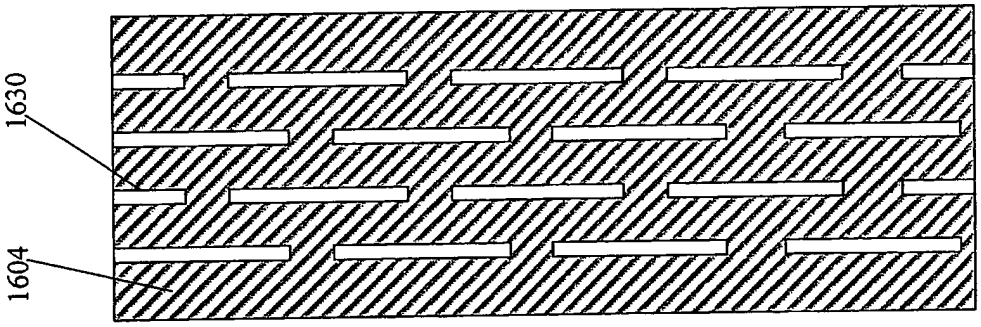


Fig. 16B

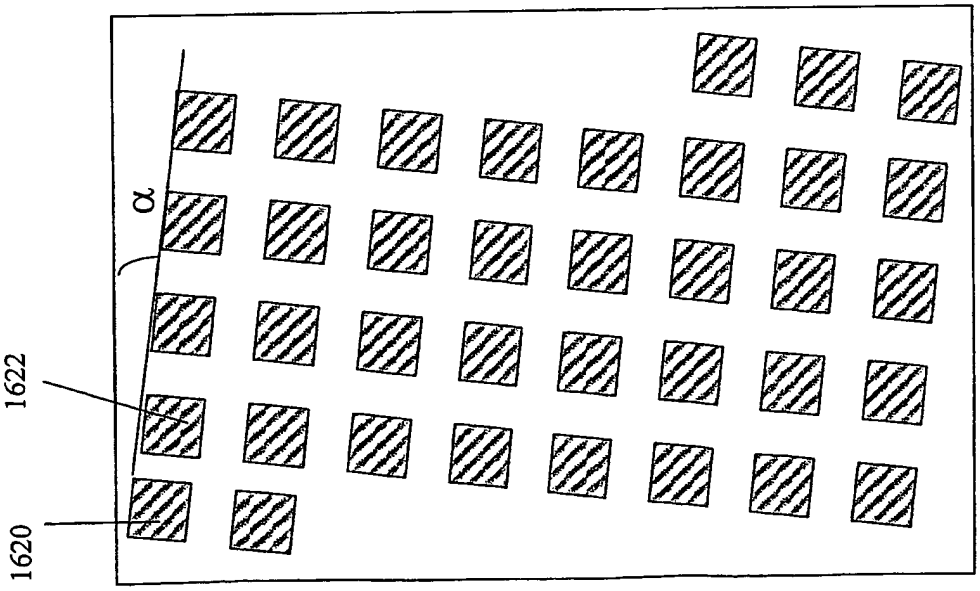


Fig. 16A

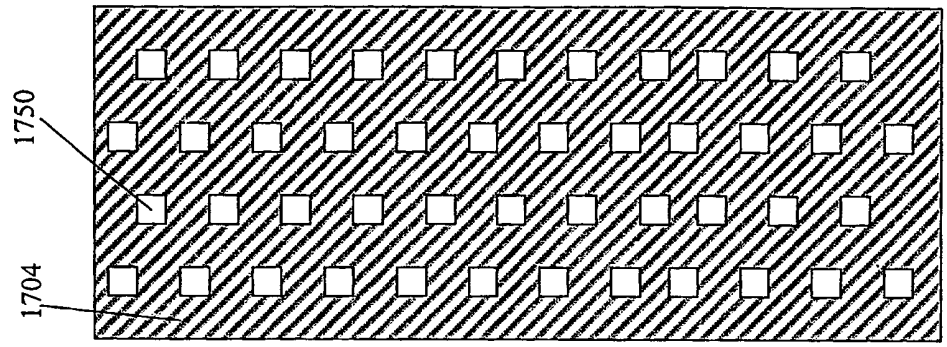


Fig. 17C

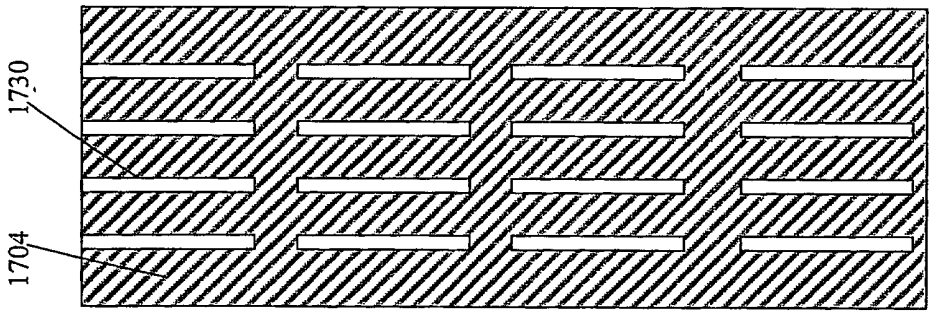


Fig. 17B

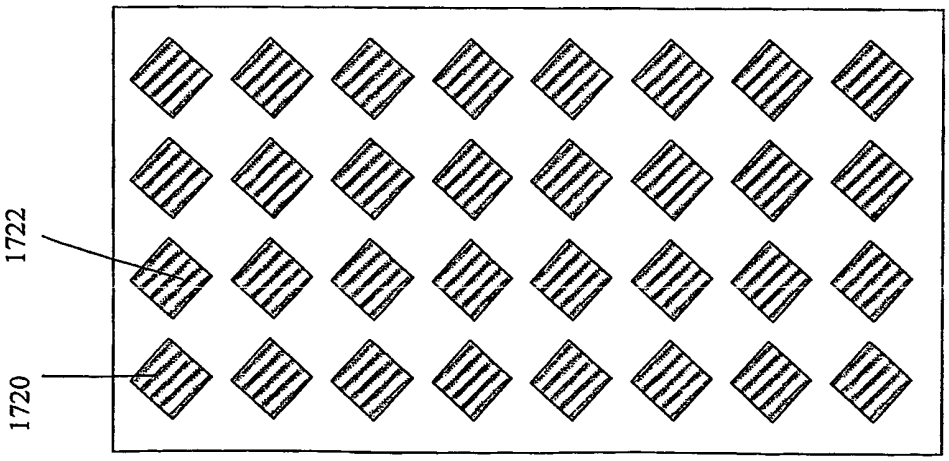


Fig. 17A

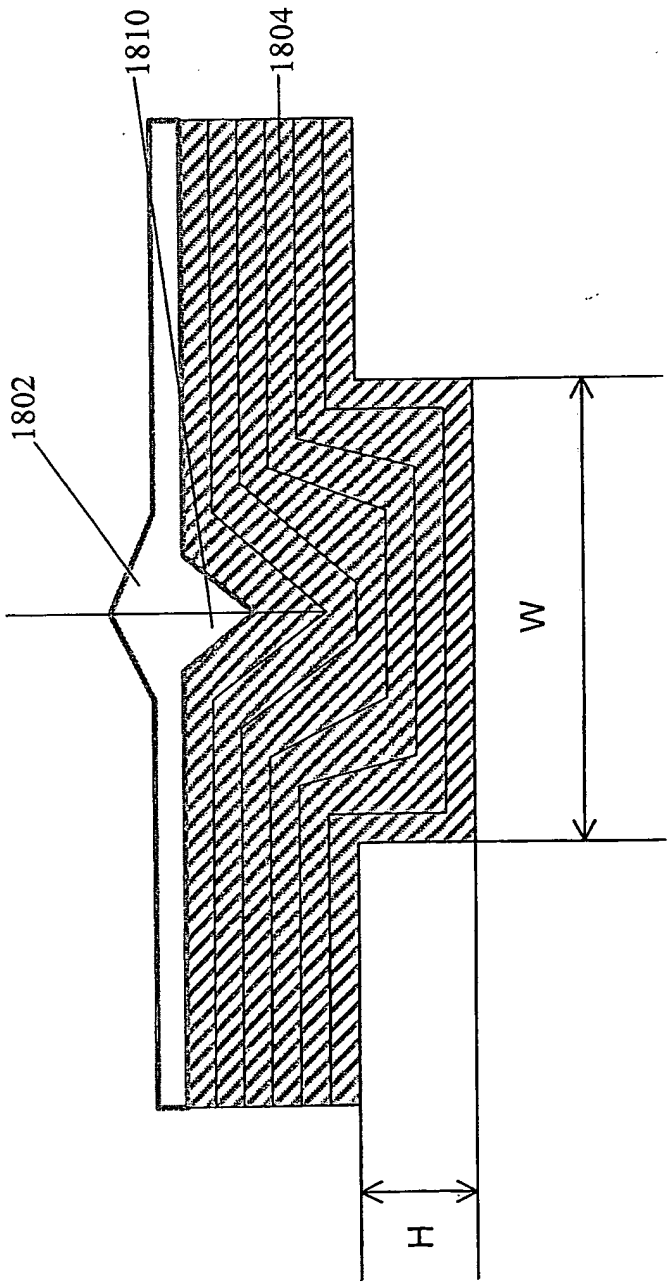


Fig. 18A

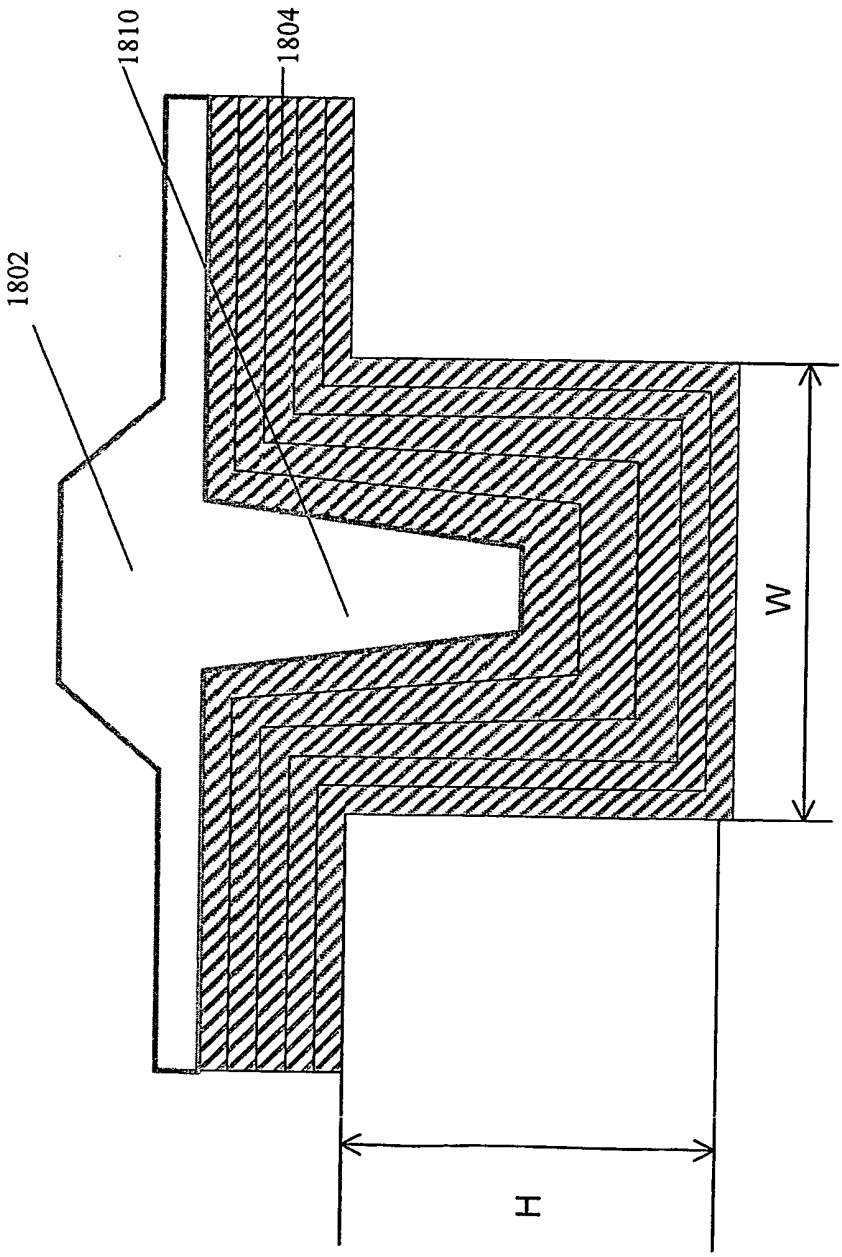


Fig. 18B

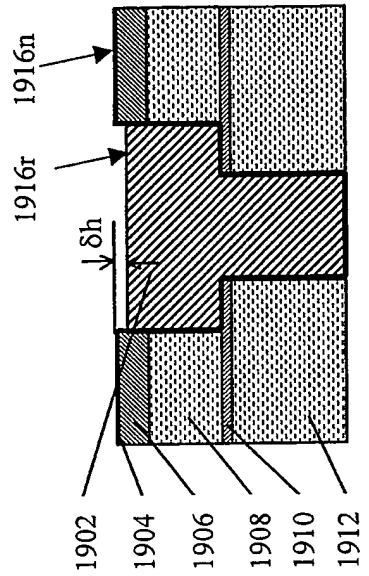


Fig. 19C

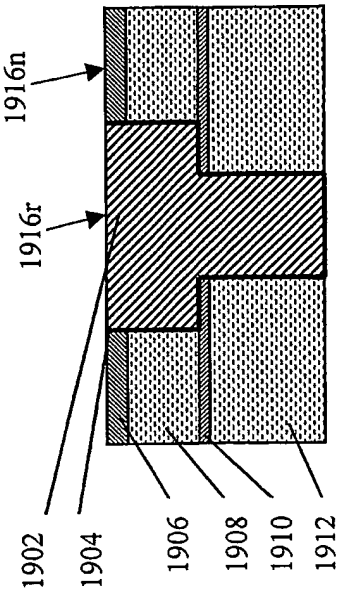


Fig. 19D

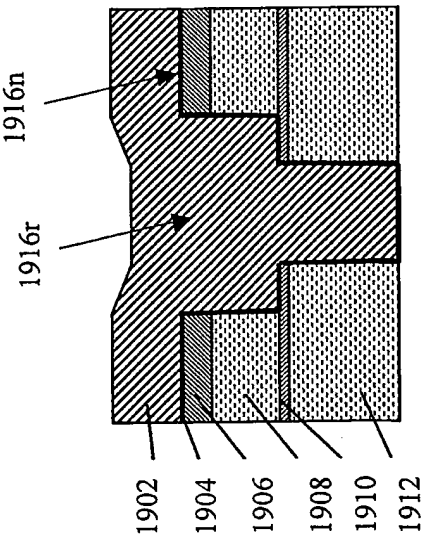


Fig. 19A

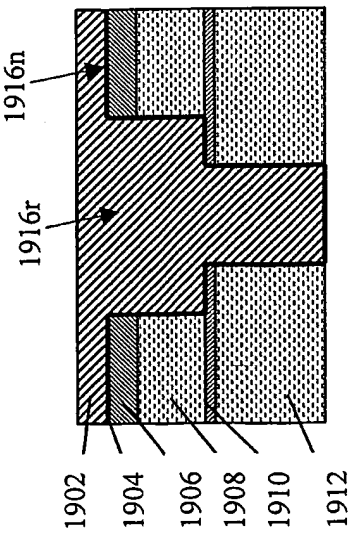


Fig. 19B

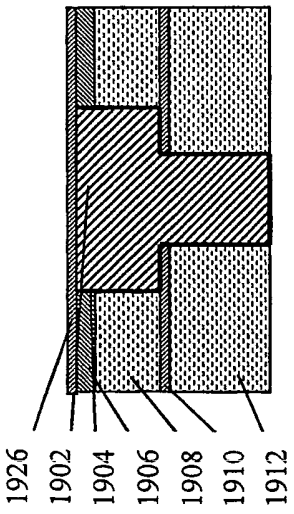


Fig. 19E

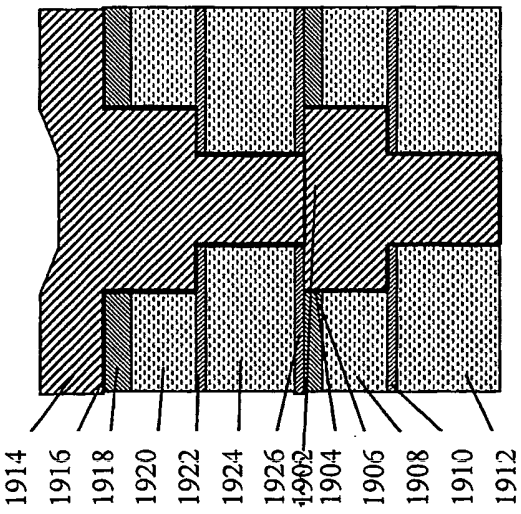


Fig. 19F

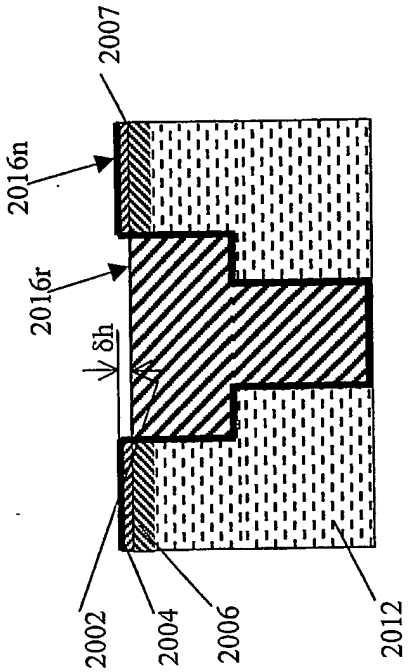


Fig. 20C

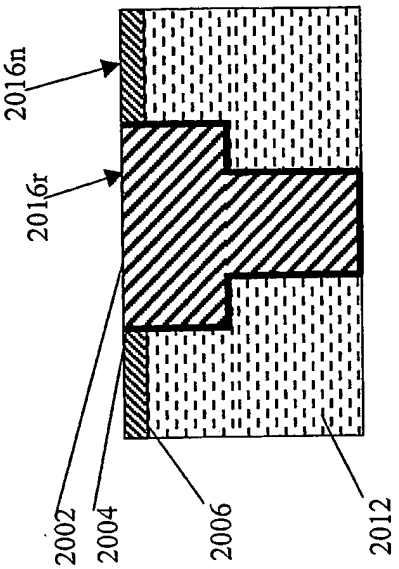


Fig. 20D

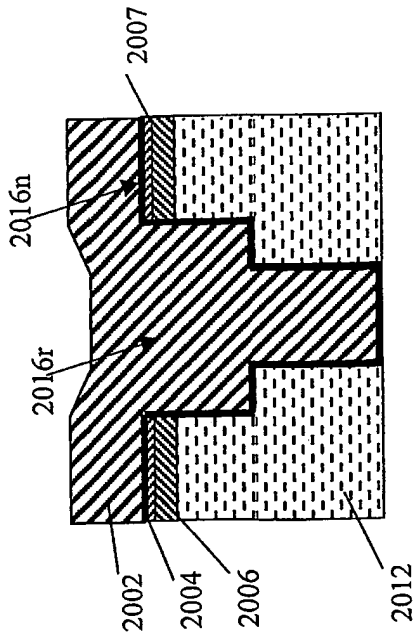


Fig. 20A

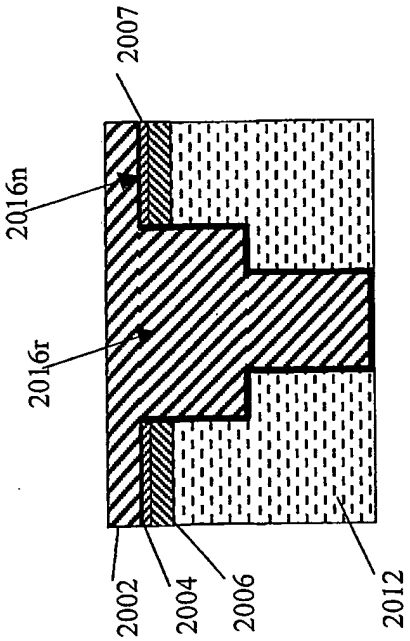


Fig. 20B

Fig. 21A

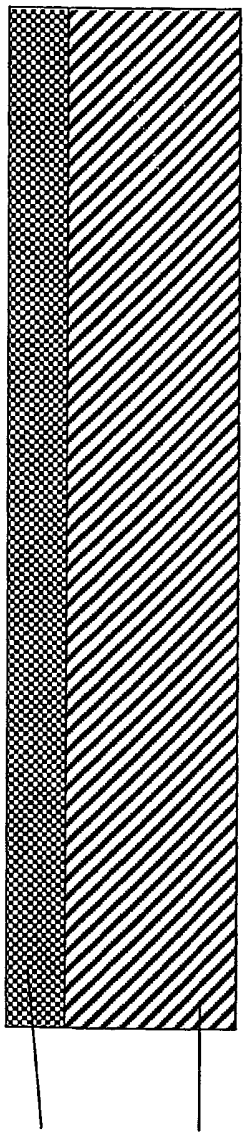


Fig. 21B

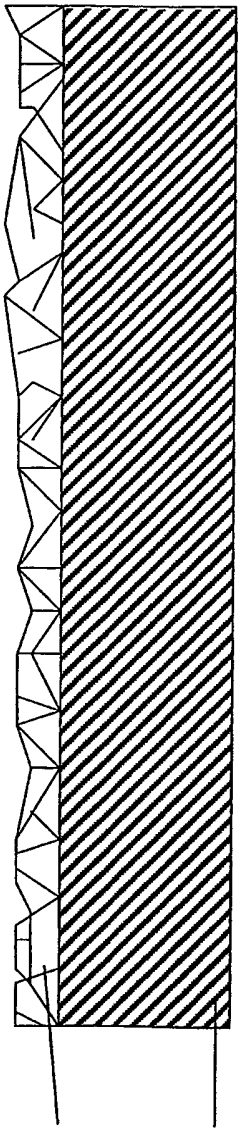


Fig. 21C

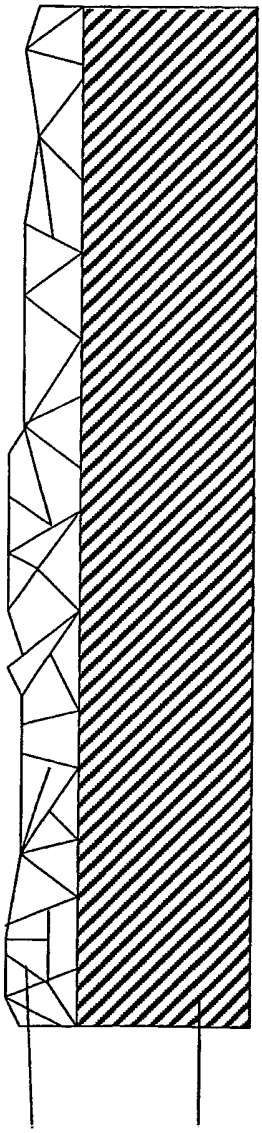
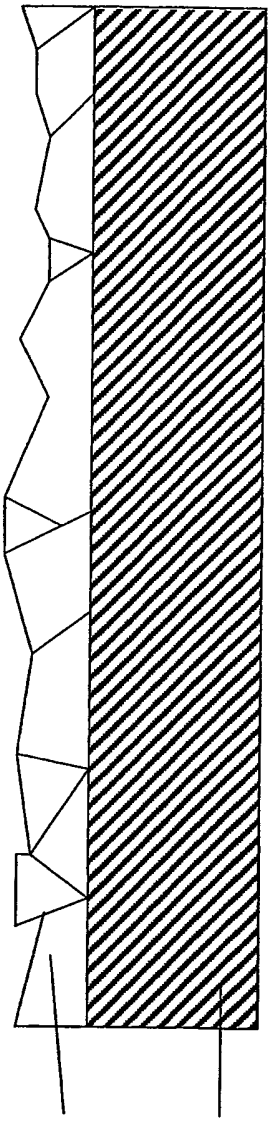


Fig. 21D



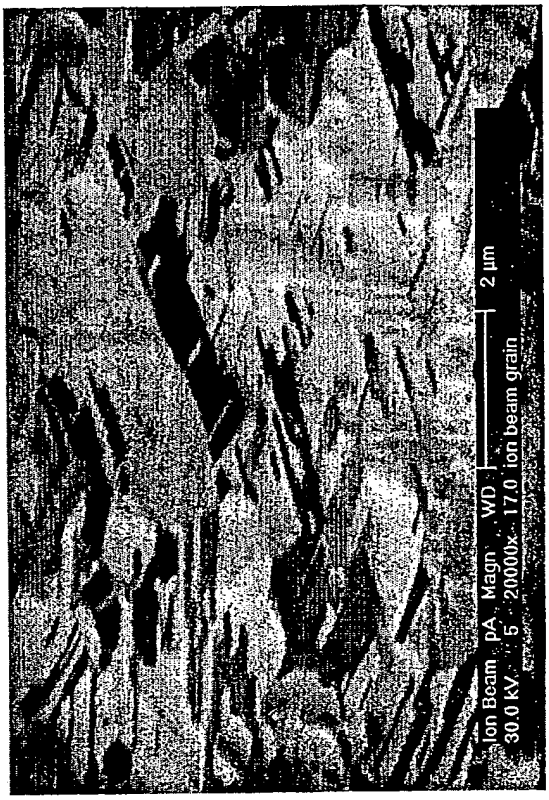


Fig. 22B

Fig. 22A

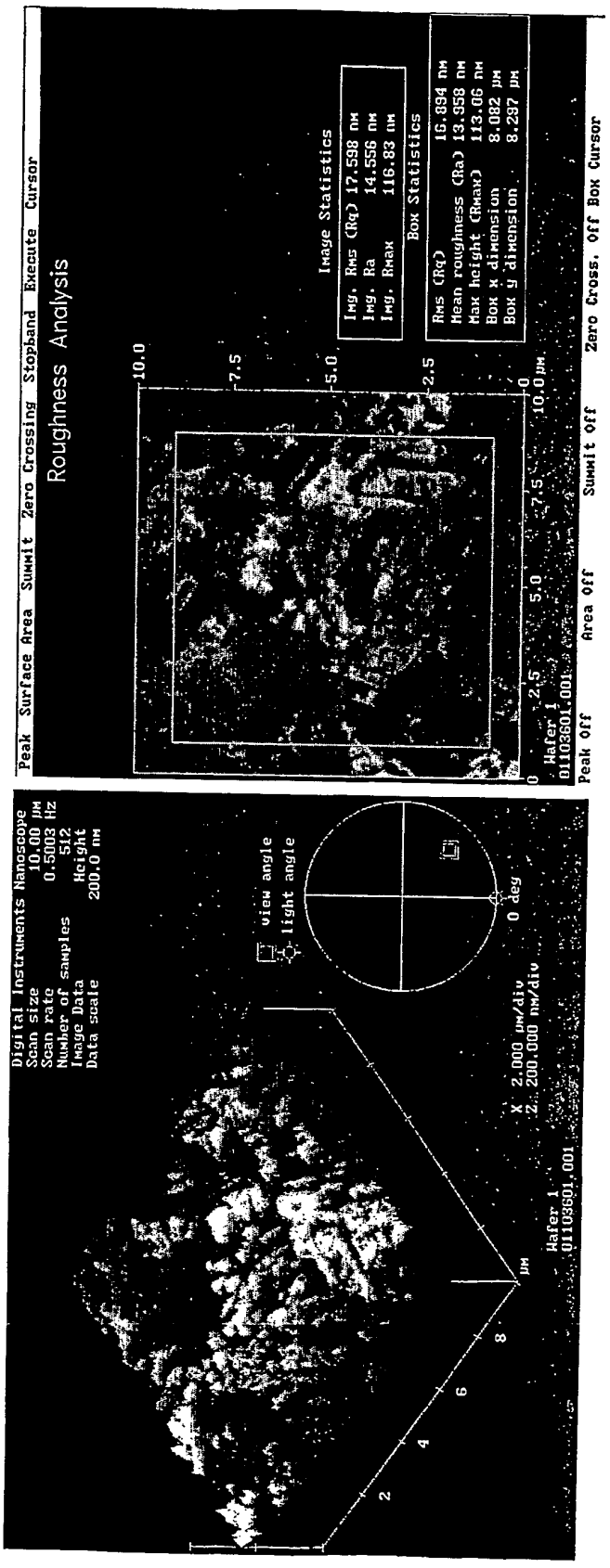

Peak Surface Area Summit Zero Crossing Stopband Execute Cursor
Roughness Analysis
Image Statistics
Img. Rms (Rq) 17.598 nm
Img. Ra 14.556 nm
Img. Rmax 116.83 nm
Box Statistics
Rms (Rq) 16.894 nm
Mean roughness (Ra) 13.958 nm
Max height (Rmax) 113.06 nm
Box x dimension 8.082 µm
Box y dimension 8.287 µm
Peak Off Area Off Summit Off Zero Cross, Off Box Cursor
Digital Instruments Nanoscope
Scan size 10.00 µm
Scan rate 0.5003 Hz
Number of samples 512
Image Data Height
Data scale 200.0 nm
view angle
light angle
0 deg
X 2.000 µm/div
Z 200.000 nm/div
Wafer 1
01103601.001

Fig. 22C

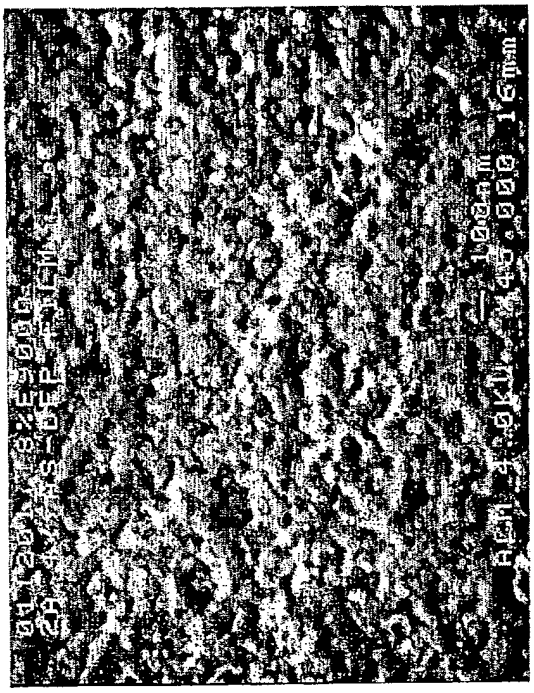


Fig. 23B

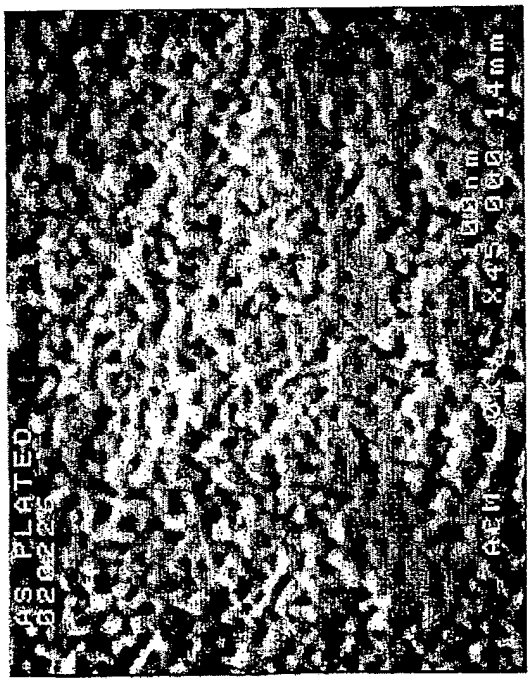


Fig. 23A

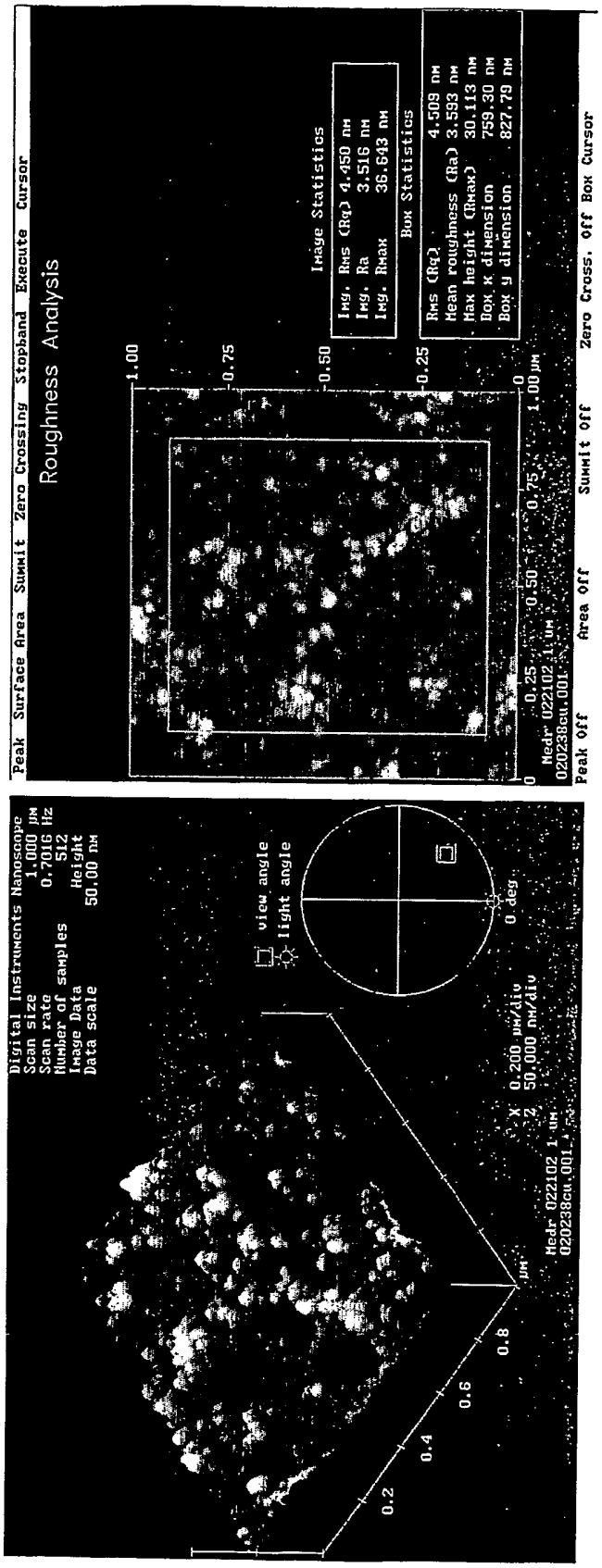

Peak Surface Area Summit Zero Crossing Stopband Execute Cursor
Roughness Analysis
Image Statistics
Img. Rms (Rq) 4.450 nm
Img. Ra 3.516 nm
Img. Rmax 36.643 nm
Box Statistics
Rms (Rq) 4.509 nm
Mean roughness (Ra) 3.593 nm
Max height (Rmax) 30.113 nm
Box x dimension 759.30 nm
Box y dimension 827.79 nm
Peak Off Area Off Summit Off Zero Cross. Off Box Cursor
Digital Instruments Nanoscope
Scan size 1.000 µm
Scan rate 0.7016 Hz
Number of samples 512
Image Data Height
Data scale 50.00 nm
view angle
light angle
0 deg
X 0.200 µm/div
Z 50.000 nm/div

Fig. 23C

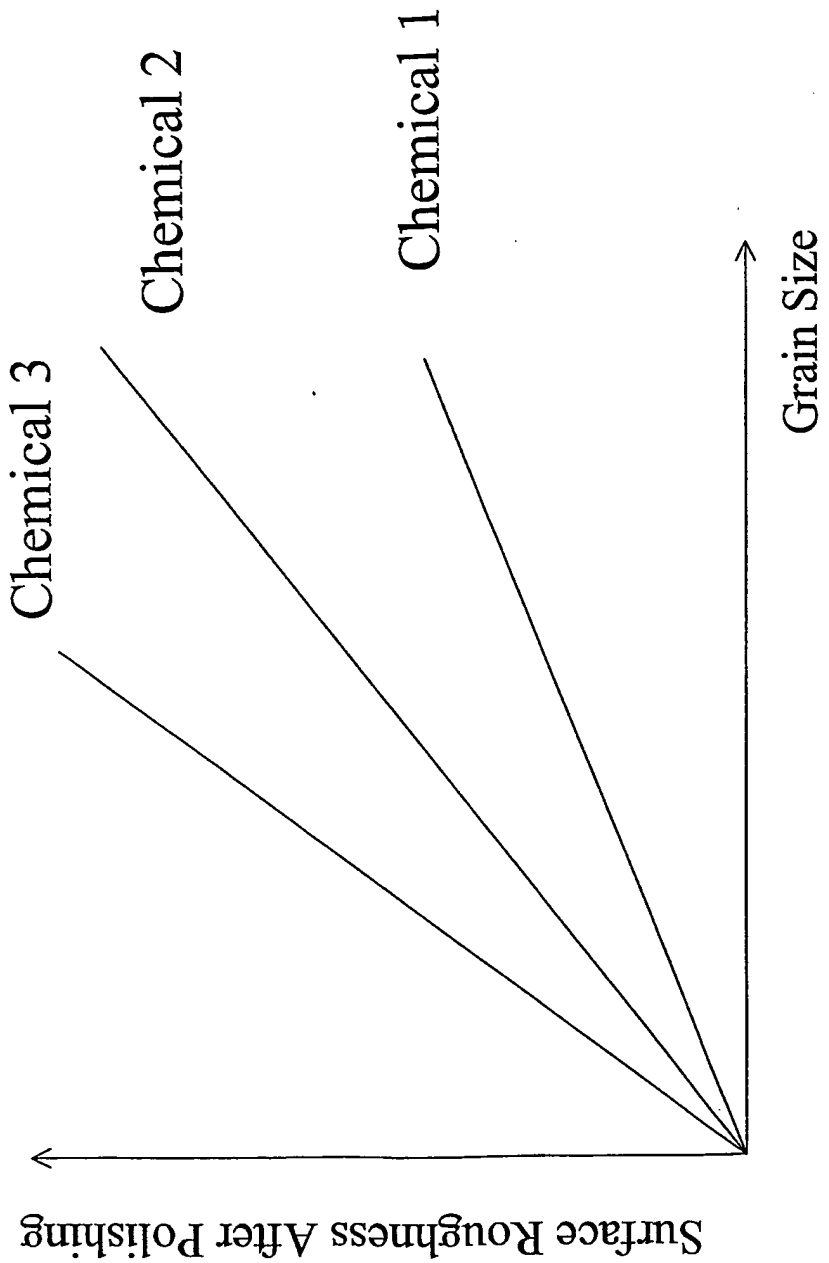

Chemical 3
Chemical 2
Chemical 1
Grain Size
Surface Roughness After Polishing

Fig. 24

Fig. 25A

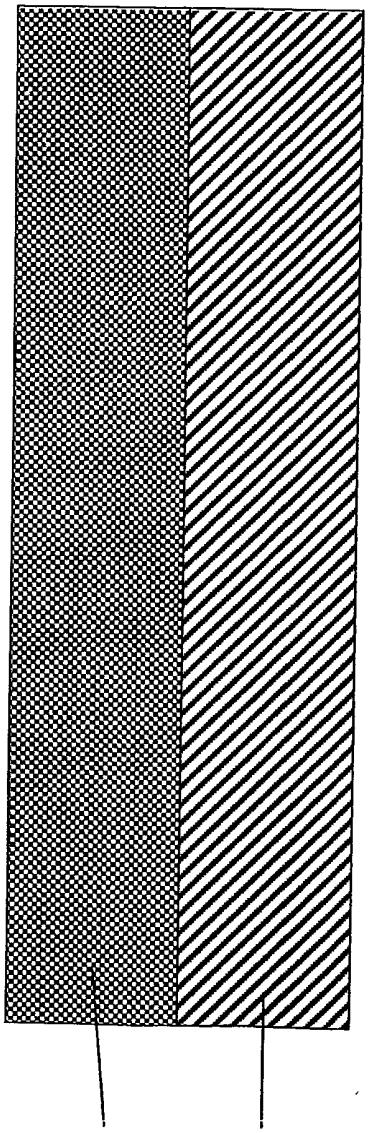


Fig. 25B

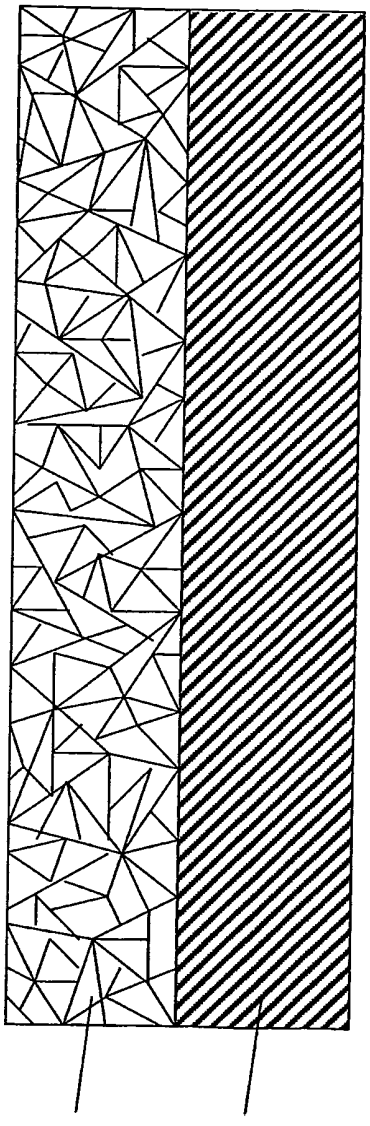


Fig. 25C

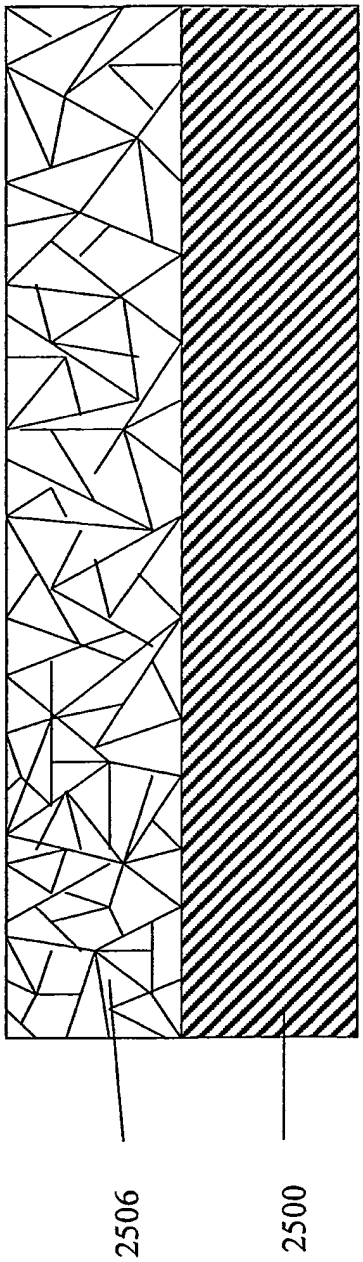
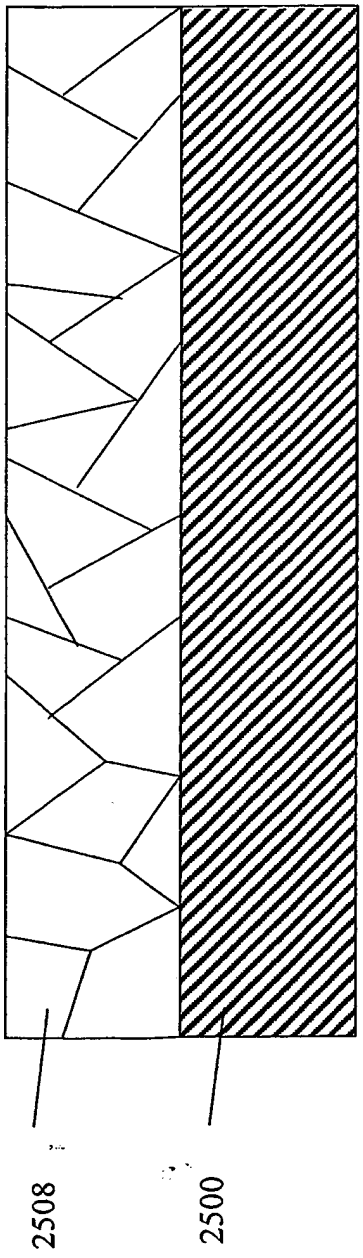


Fig. 25D



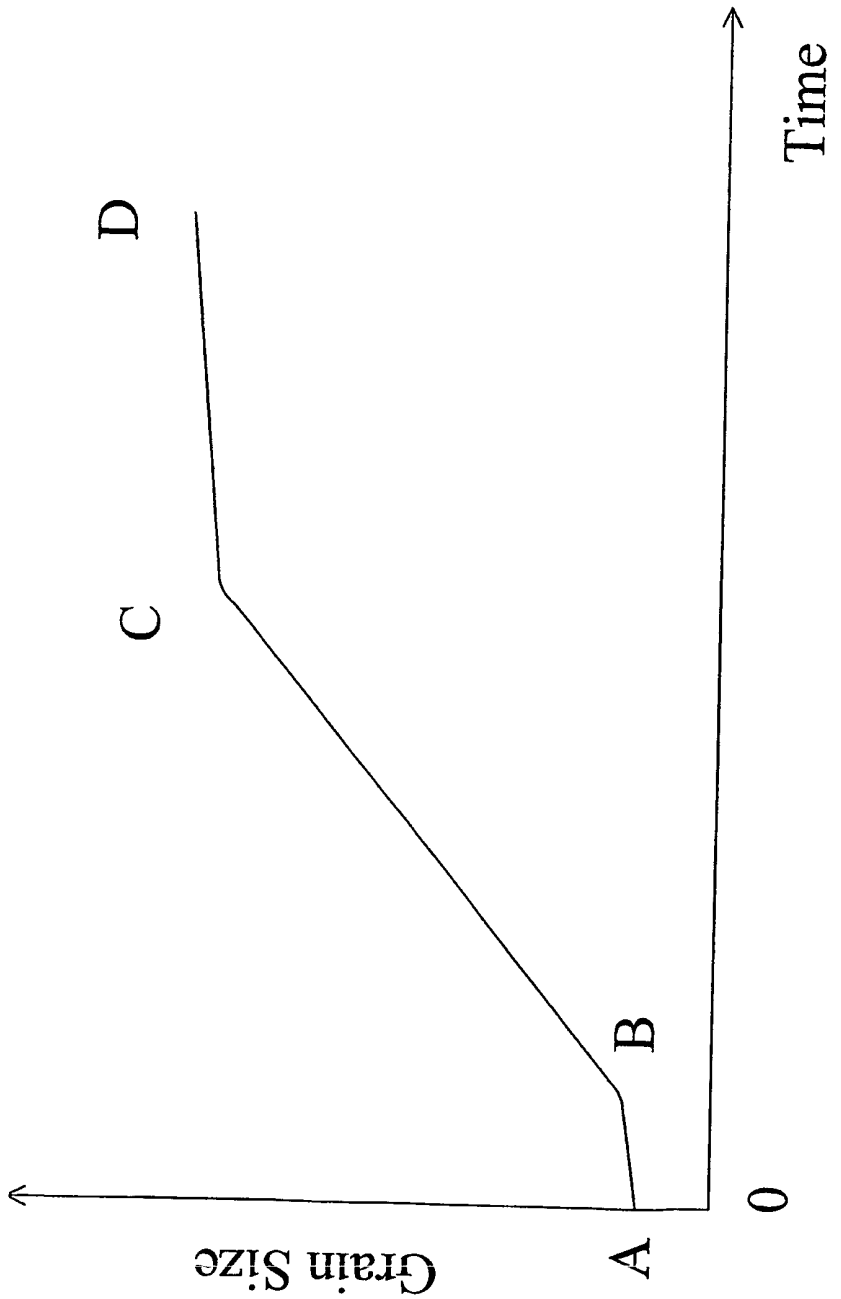


Fig. 26

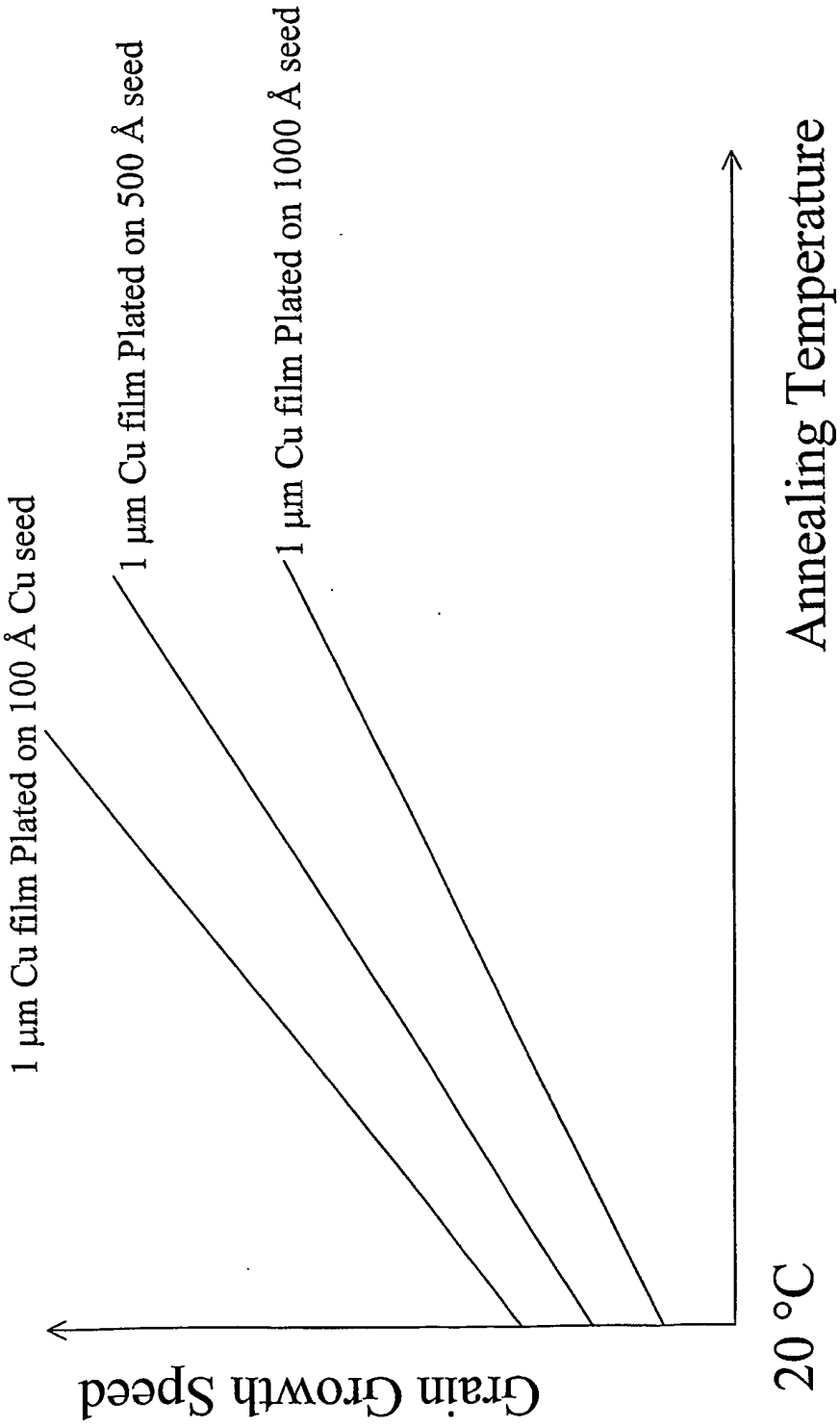

1 µm Cu film Plated on 100 Å Cu seed
1 µm Cu film Plated on 500 Å seed
1 µm Cu film Plated on 1000 Å seed
Grain Growth Speed
20 °C
Annealing Temperature

Fig. 27

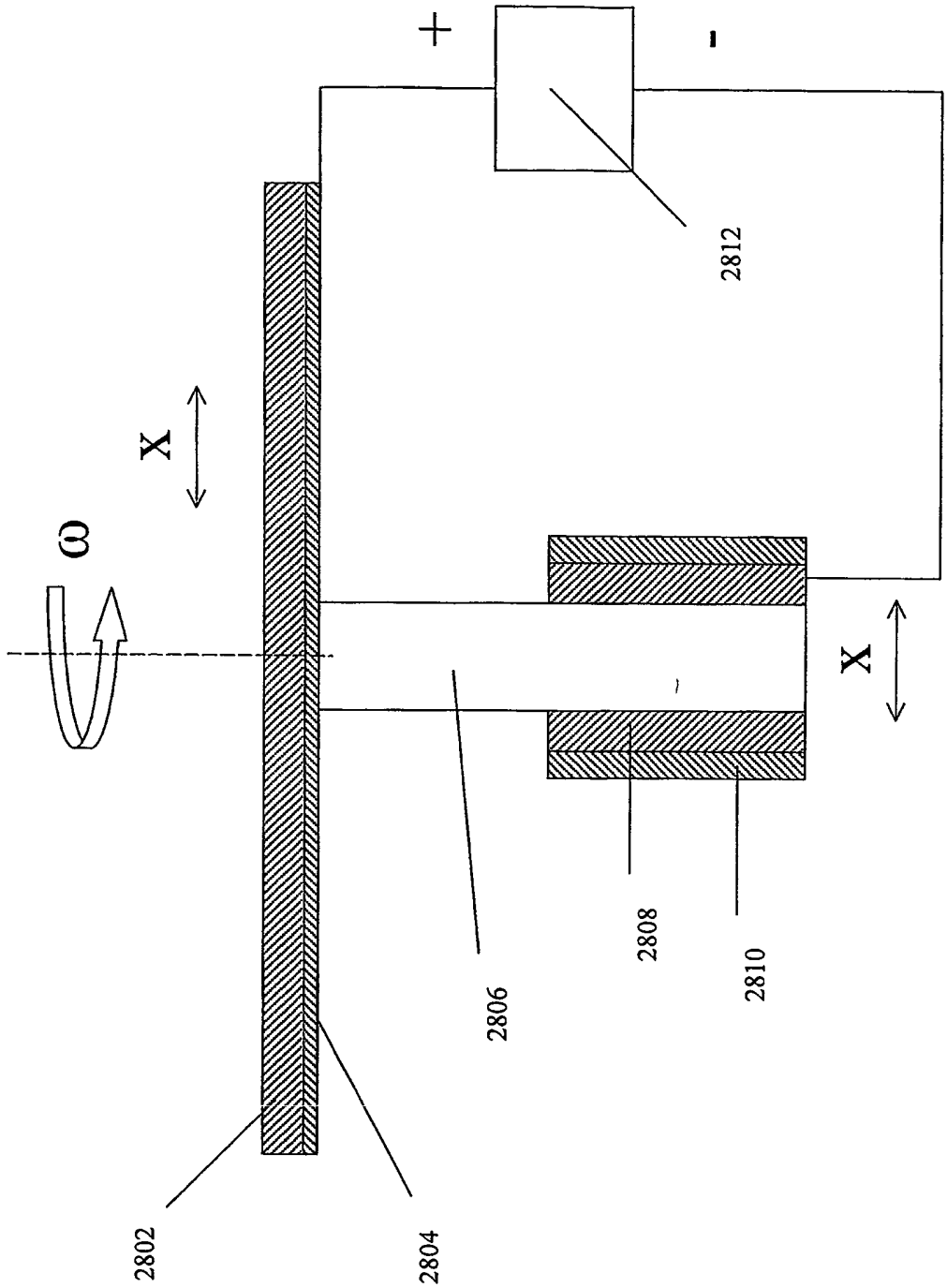


Fig. 28A

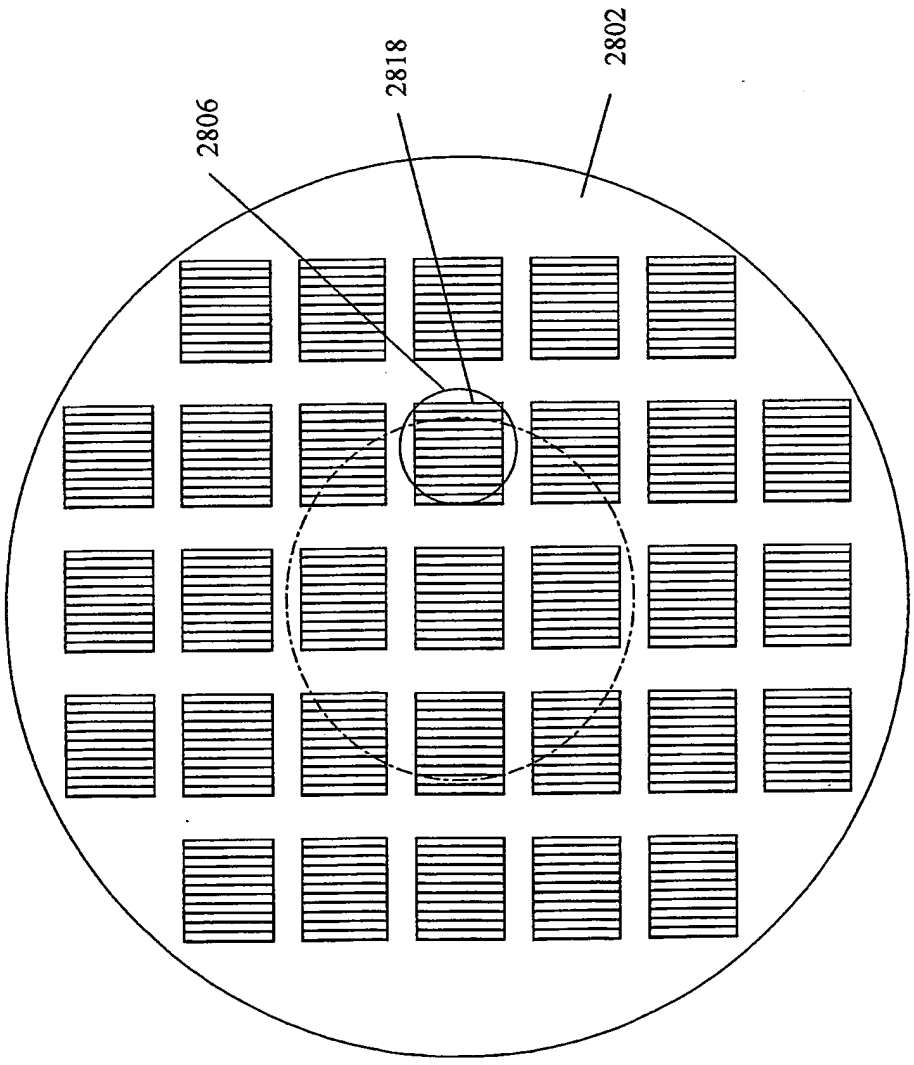


Fig. 28B

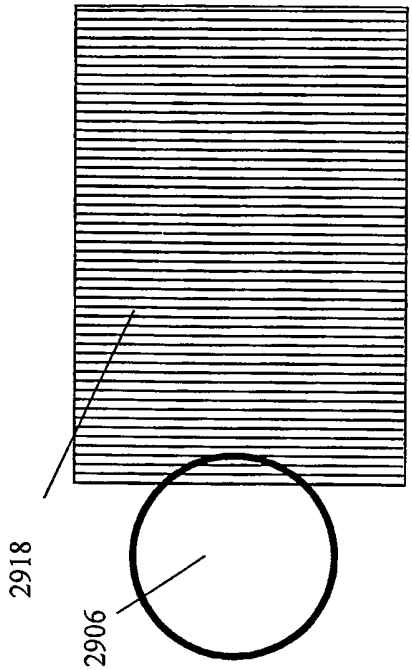


Fig. 29B

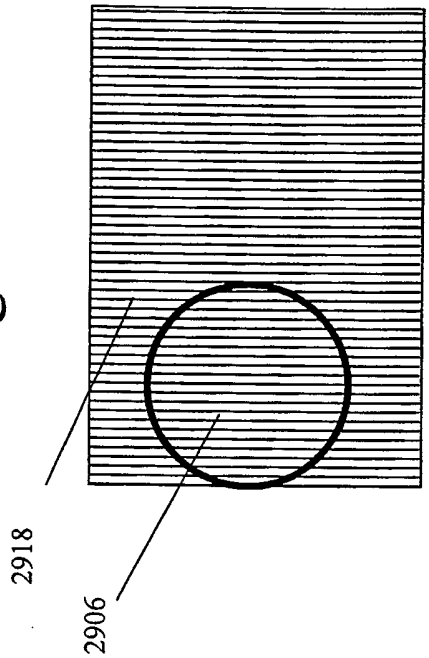


Fig. 29D

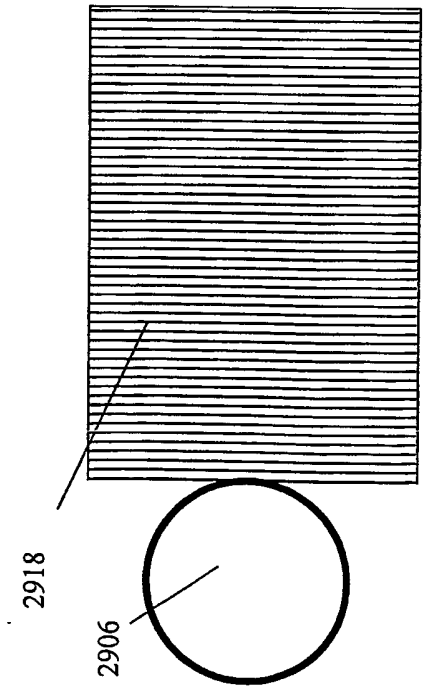


Fig. 29A

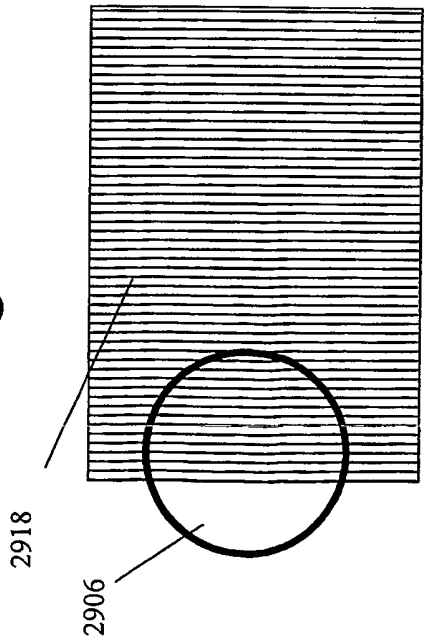


Fig. 29C

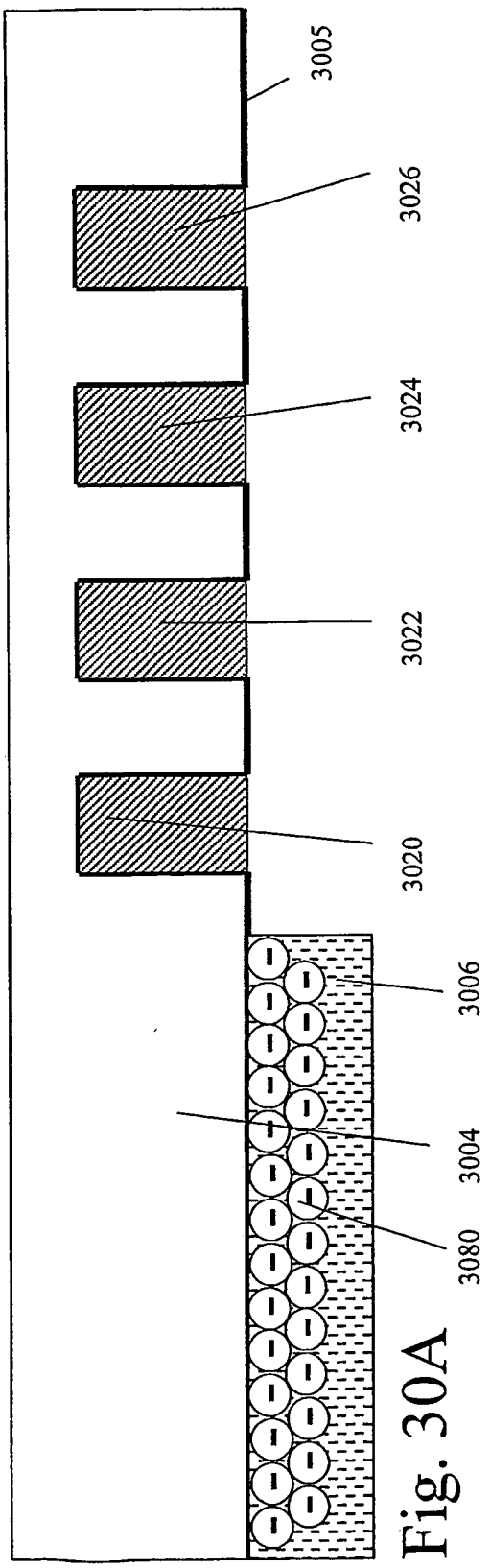


Fig. 30A

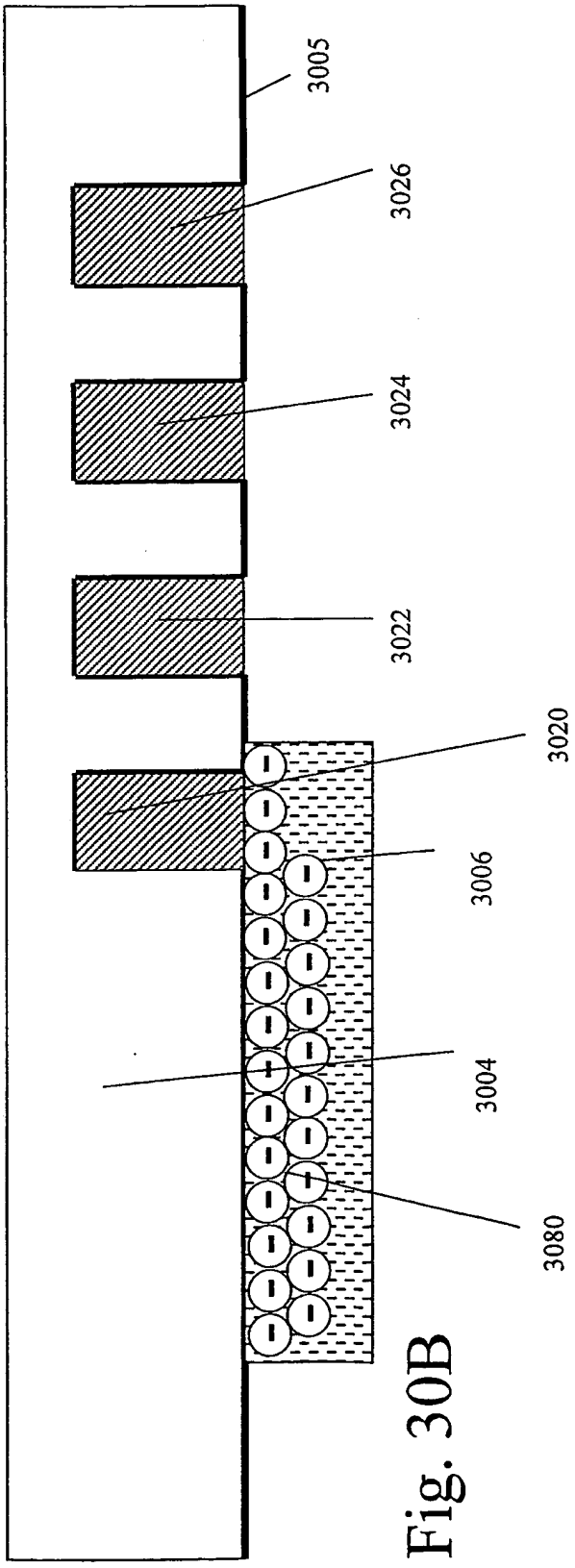


Fig. 30B

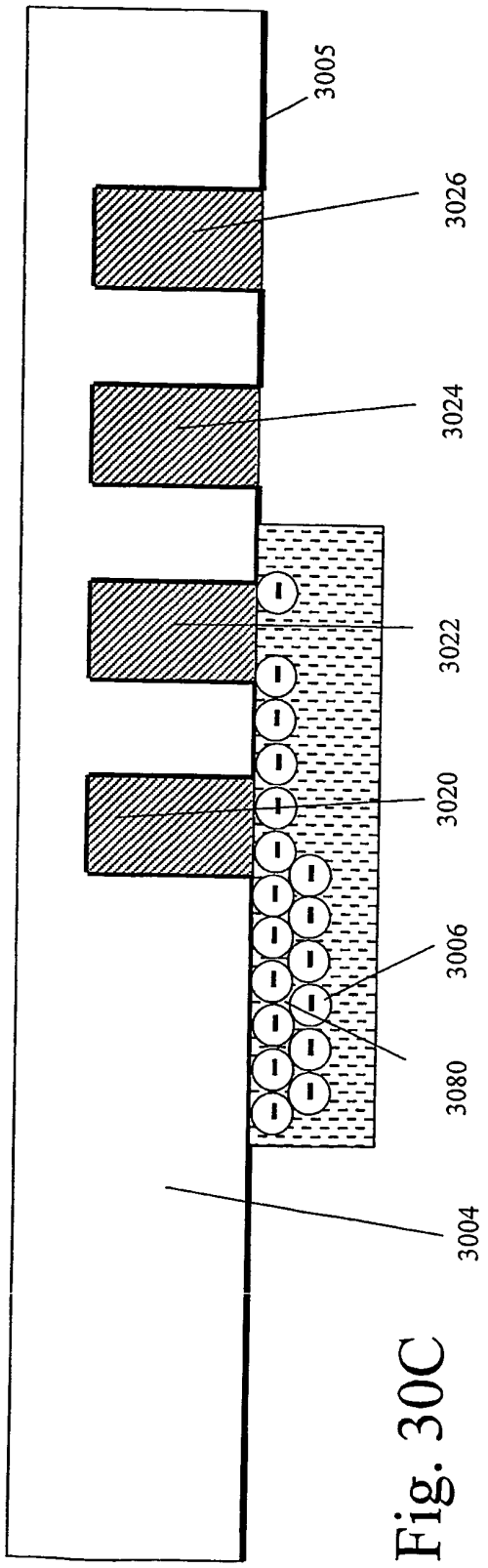


Fig. 30C

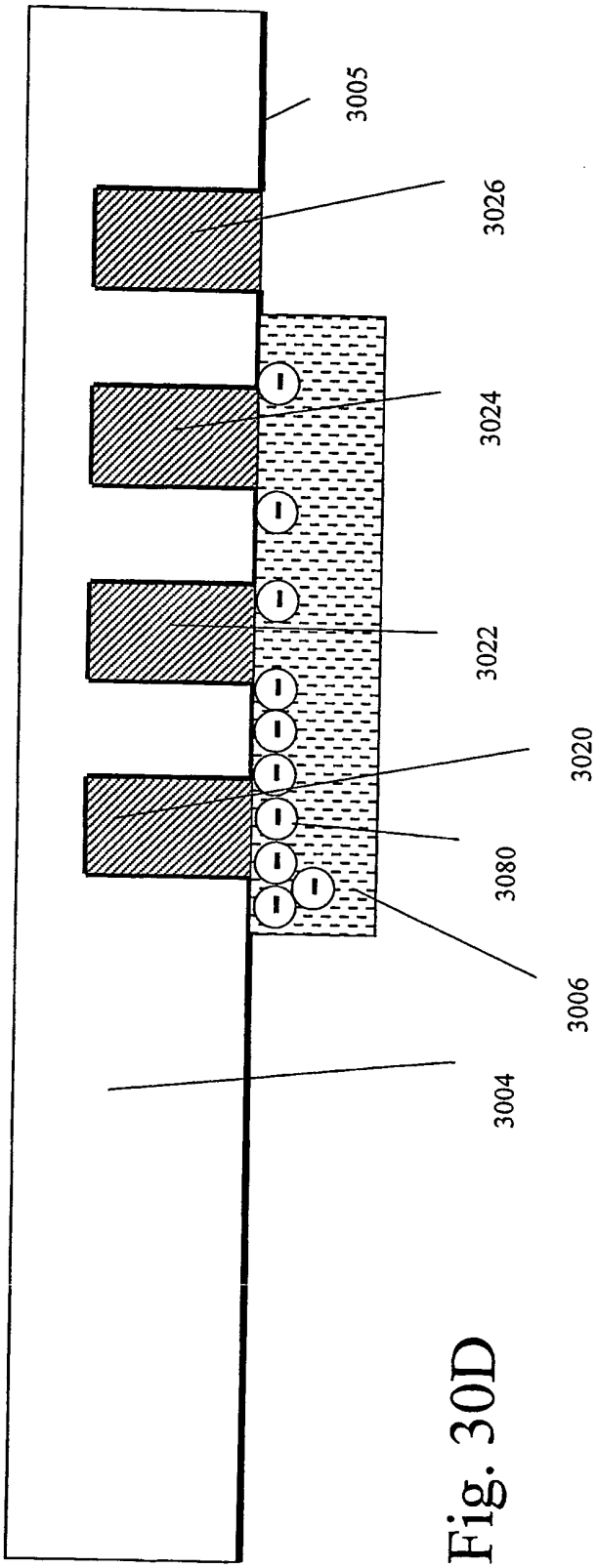


Fig. 30D

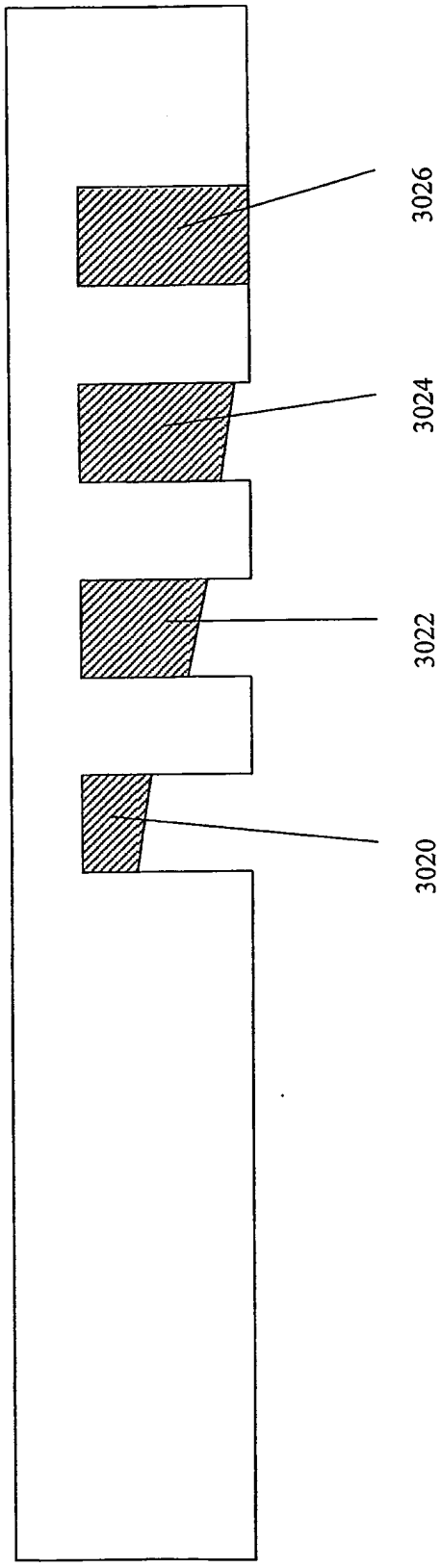


Fig. 30E

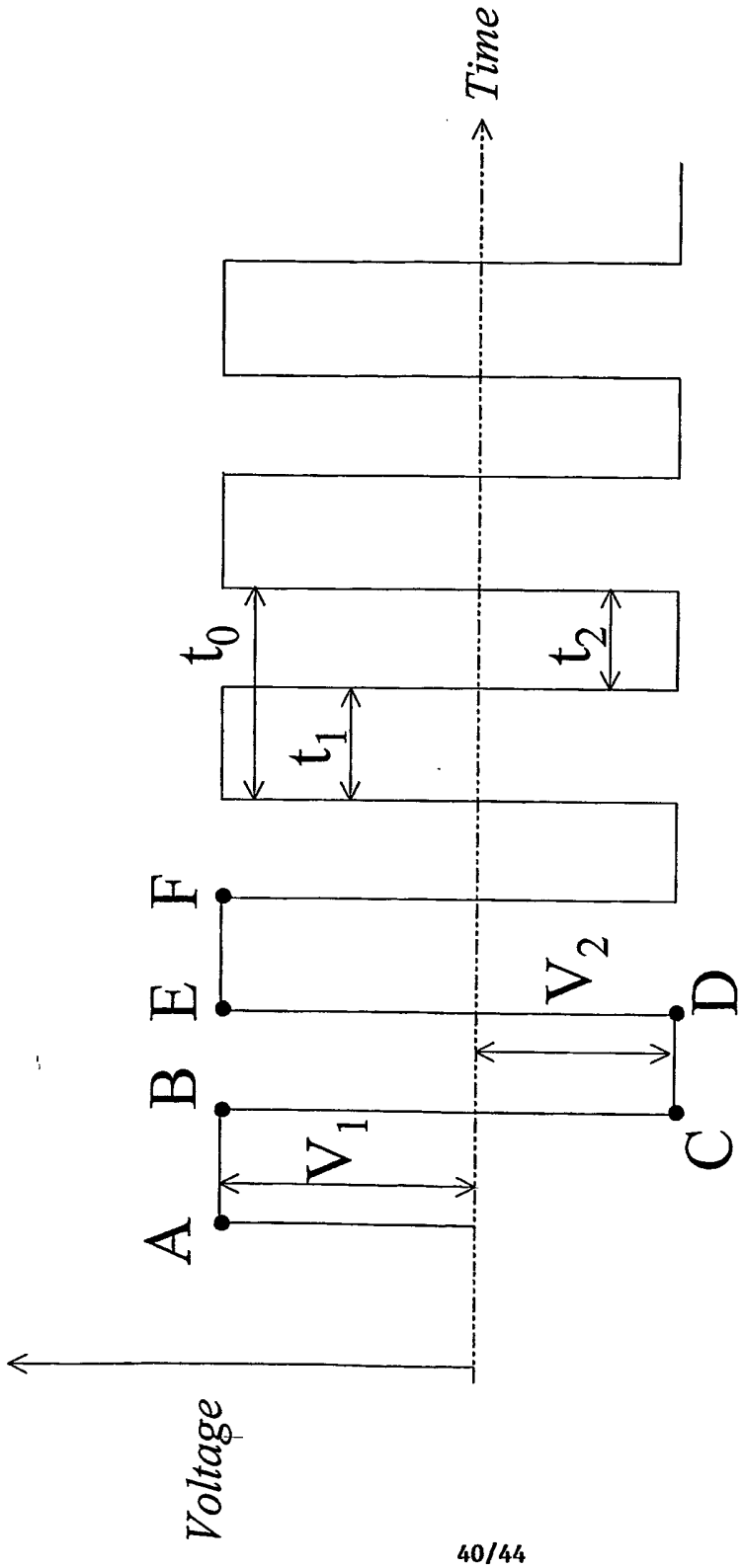


Fig. 31

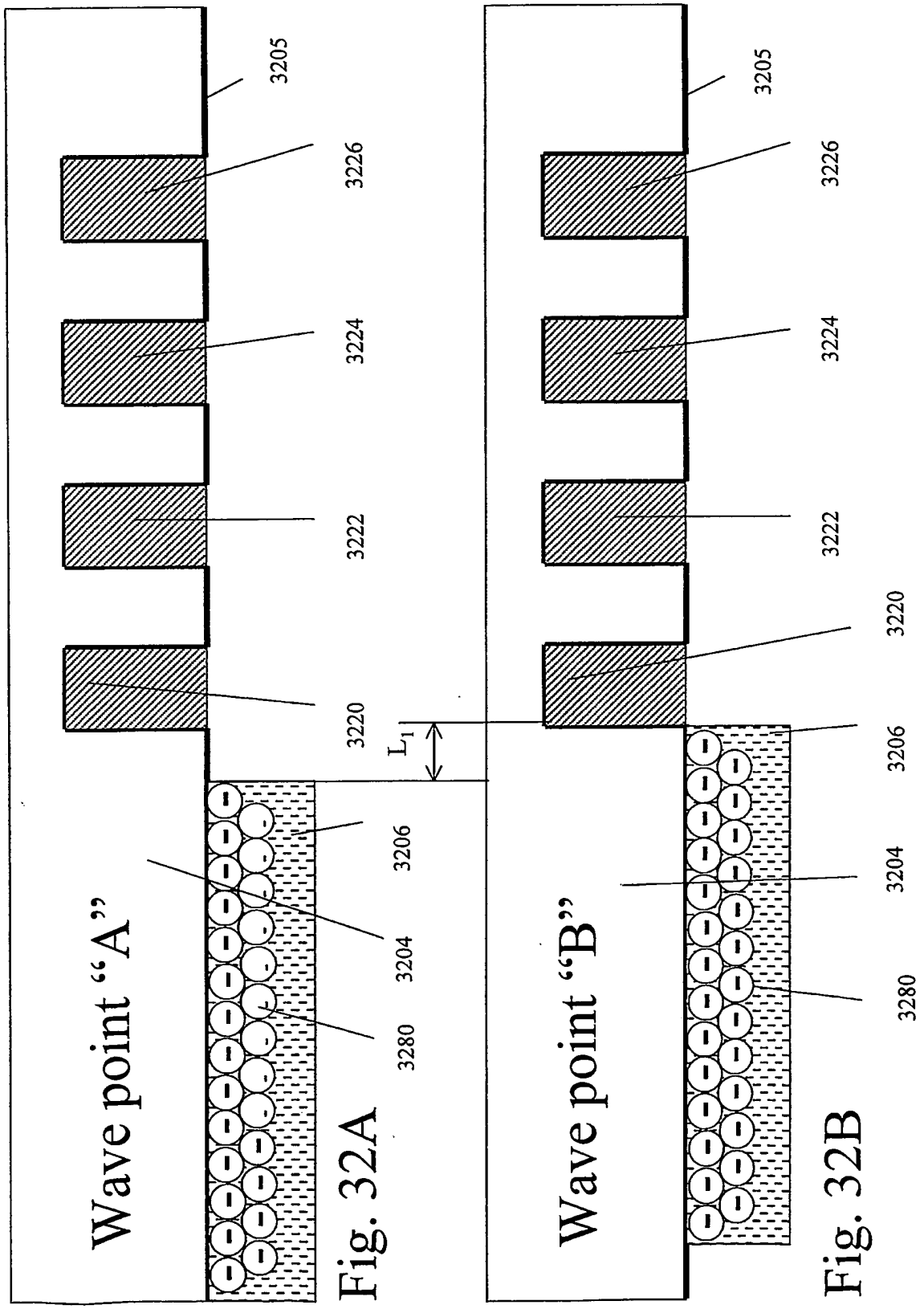


Fig. 32A

Fig. 32B

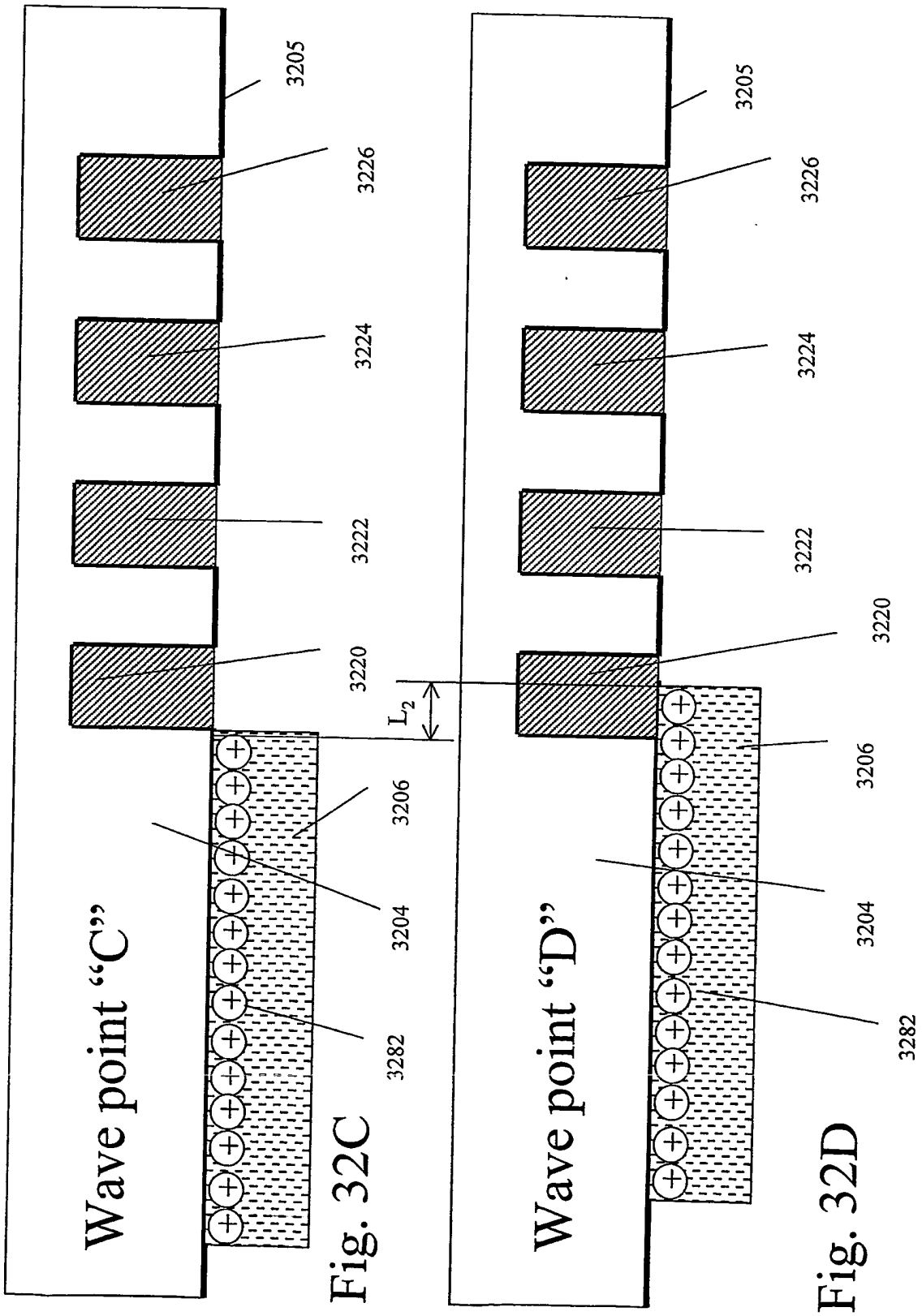


Fig. 32C

Fig. 32D

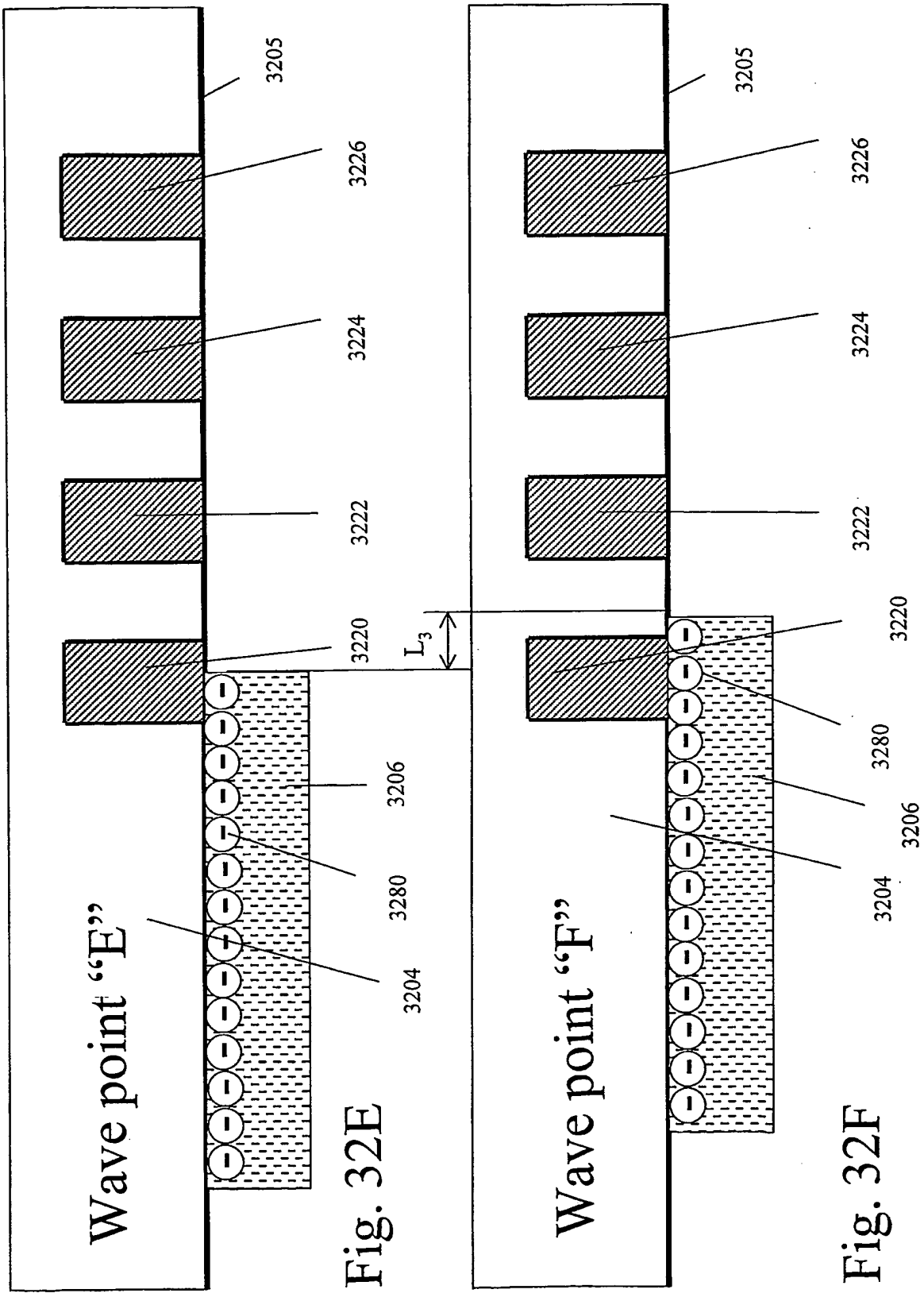


Fig. 32E

Fig. 32F

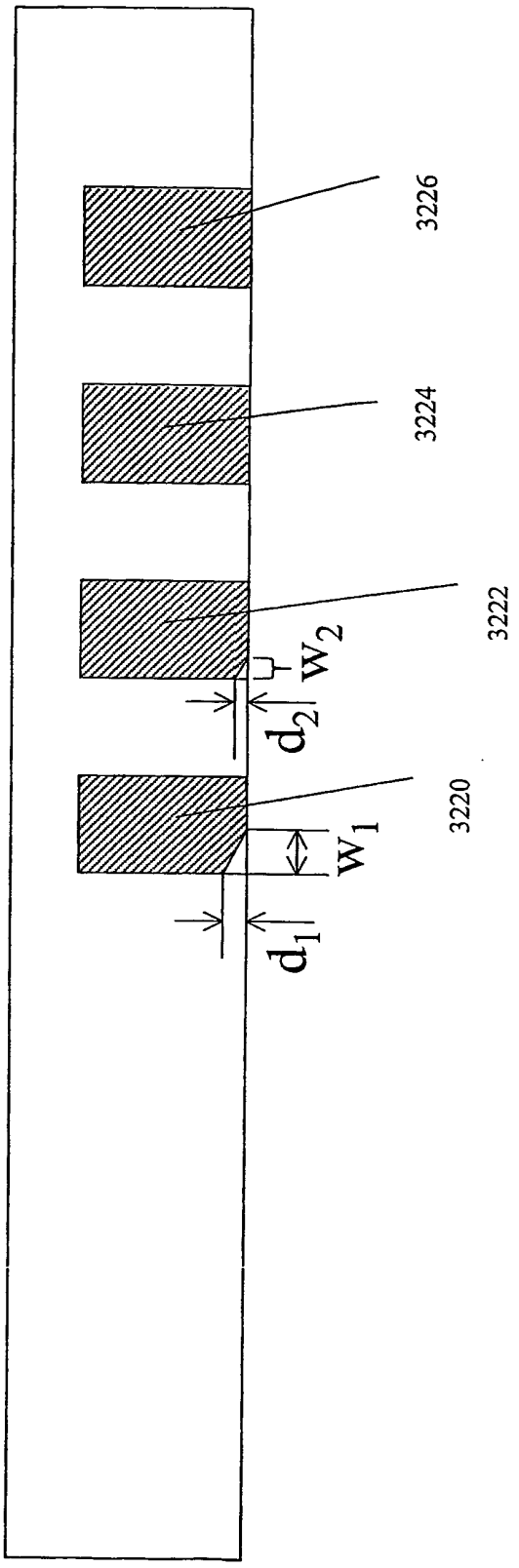


Fig. 32G